

Compal

EL5C3/EL531/EL431

DIS M/B Schematic Document

Intel Whiskey Lake Processor with DDR4

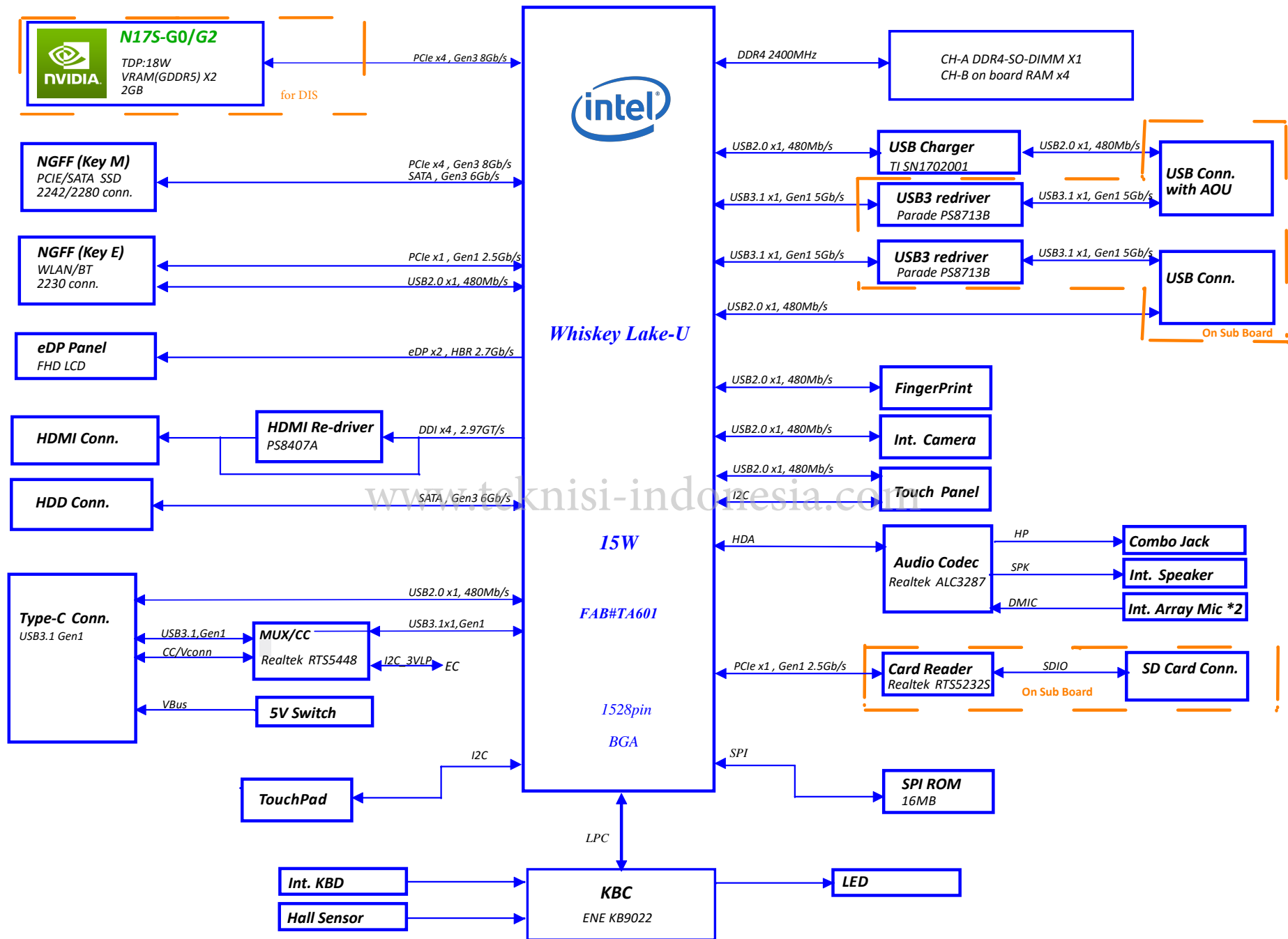
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2018-09-20

LA-H101P

REV: 0.A (EVT)

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Voltage Rails

power plane	B+	+5VALW +3VALW +1.8VALW +1.05VALW	+1.2V +2.5V	+5VS +3VS +VCCPLL_OC +1.05VS_VCCSTG +VCC_CORE +VCC_GT +VCC_SA +1.05V_VCCIO +1.8VS +0.6VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

BOM Structure Table

Item	BOM Structure
DIS Only Components	DIS@
UMA Only Components	UMA@
HDMI Logo	45@
Touch Screen	TS@
Memory Down - SDP Package	SDP@
Memory Down - DDP Package	DDP@
GPU GC6 Components	GC6@
Un-Mount GPU GC6 Components	NOGC6@
Connectors	ME@
Intel CNVi	CNVi@
EMI Category	EMI@
ESD Category	ESD@
RF Category	RF@
Test Point	TP@
Keyboard BackLight	KBL@ NOKBL@
Project select	S540@ S340@ C340@ S340_14@ S340_15@ N17S_G1@ N17S_G0@ N16V@ N16S@ N16@ N17@
GPU select	MD@ NO_MD@
MIC select	Arrary_MIC@ Single_MIC@
TypeC 20V_PRTCT	20V_PRTCT@

Item	BOM Structure
S340_15 MD (Hynix 4GB)	H4G_S340_15@
S340_15 MD (Micron 4GB)	M4G_S340_15@
S340_15 MD (Samsung 4GB)	S4G_S340_15@
C340 MD (Hynix 4GB)	H4G_C340@
C340 MD (Micron 4GB)	M4G_C340@
C340 MD (Samsung 4GB)	S4G_C340@
On Board RAM X76 Resistors	X76RAM@
S340_15@ VRAM (Hynix 2GB)	VH2G_S340_15@
S340_15@ VRAM (Micron 2GB)	VM2G_S340_15@
S340_15@ VRAM (Samsung 2GB)	VS2G_S340_15@
C340 VRAM (Hynix 2GB)	VH2G_C340@
C340 VRAM (Micron 2GB)	VM2G_C340@
C340 VRAM (Samsung 2GB)	VS2G_C340@
S340_14 MD (Hynix 4GB)	H4G_S340_14@
S340_14 MD (Micron 4GB)	M4G_S340_14@
S340_14 MD (Samsung 4GB)	S4G_S340_14@
S340_14@ VRAM (Hynix 2GB)	VH2G_S340_14@
S340_14@ VRAM (Micron 2GB)	VM2G_S340_14@
S340_14@ VRAM (Samsung 2GB)	VS2G_S340_14@

USB 2.0 Port Table

Port	External USB Port
1	USB2/3 Port (IO - 1)
2	USB2/3 Port (IO - 2)
3	USB2/3 Port (Type-C)
4	Touch Screen
5	
6	Camera
7	Fingrt Print
8	
9	
10	NGFF WLAN+BT

USB 3.0 Port Table

Port	External USB Port
1	USB2/3 Port (IO - 1)
2	USB2/3 Port (IO - 2)
3	USB2/3 Port (Type-C)
4	
5	
6	

PCIe Port Table

Port	Lane	
1		
2		
3		
4	0	DGPU
5	0	
6	1	
7	2	
8	3	
9	1	CardReader
10	0	
11		NGFF WLAN+BT
12	0	
13	3	SSD
14	2	
15	1	
16	0	

SATA Port Table

Port	External SATA Port
0	
1A	HDD
1B	SSD1

EC SM Bus1 address

EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011x 16h	NCT7718W	1001 100x 98h

PCH SM Bus address

GPU SM Bus address

Device	Address	Device	Address
DDR_JDIMM1 Touch Pad	1010 000x A0h	Internal thermal sensor	1001 111x 9Eh

SMBUS Control Table

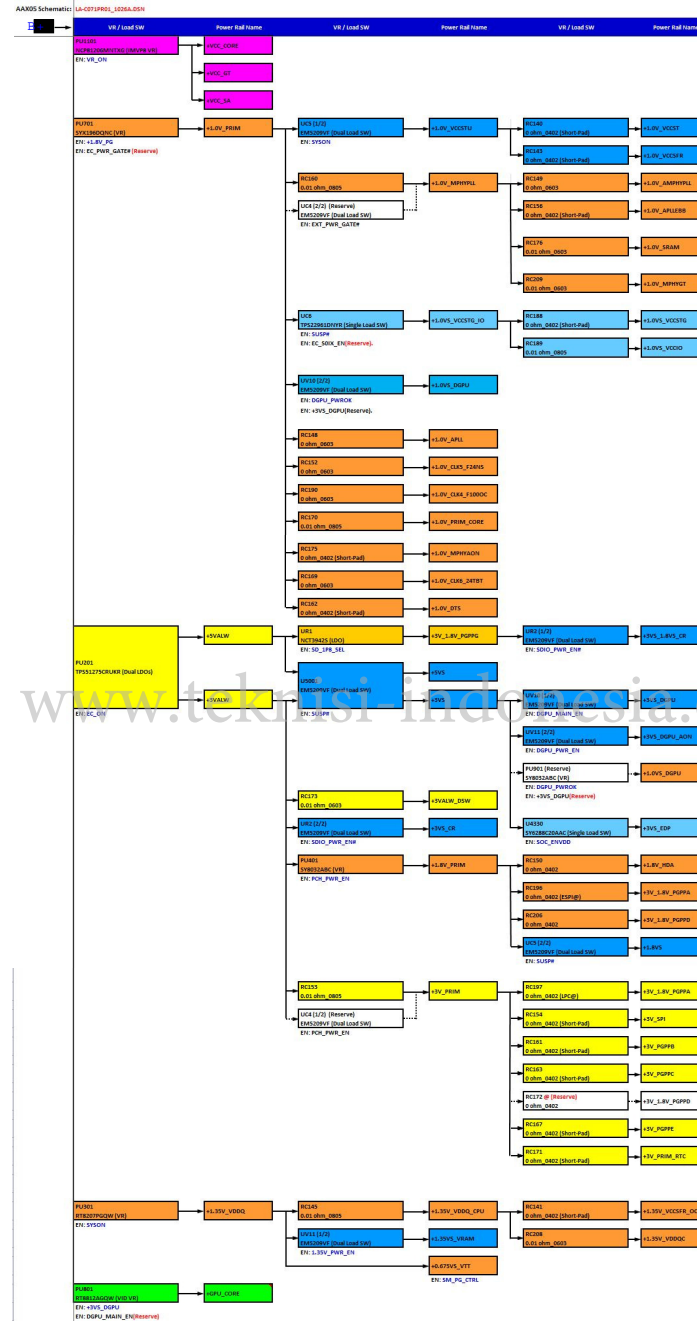
	SOURCE	DGPU	BATT	CHARGER	NECP388	SODIMM	TP	PCH	G-SENSOR	THM sensor
EC_SMB_CK1	NECP388 +3VL	X	+3VALW	+19V_VIN	X	X	X	X	X	X
EC_SMB_DA1										
EC_SMB_CK2	NECP388 +3VS	X	X	X	+3VS	X	X	+3VS	X	+3VS
EC_SMB_DA2										
EC_SMB_CK4	NECP388 +3VS	X	X	X	X	X	X	X	+3VS	X
EC_SMB_DA4										
SOC_SMBCLK	PCH +3VALW	X	X	X	X	+3VS	+3VS	X	X	X
SOC_SMBDATA										
SOC_SMLCLK	PCH +3VALW	X	X	X	X	X	X	X	X	X
SOC_SMLDATA										
EC_SMB_CK2	PCH +3VS	X	X	X	+3VS	X	X	X	X	X
EC_SMB_DA2										

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

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-PowerMap_DDR4_Volume_NON CSJ



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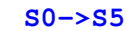


Table 5-13. DDI Disabling and Termination Guidelines

Port	Strap	How to Enable Port?	How to Disable Port?
Port 1	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm $\pm 5\%$ resistor	No Connect
Port 2	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm $\pm 5\%$ resistor	
Port 3	DDPD_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm $\pm 5\%$ resistor	
Port 4	DDPF_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm $\pm 5\%$ resistor	

< Compensation PU For eDP >

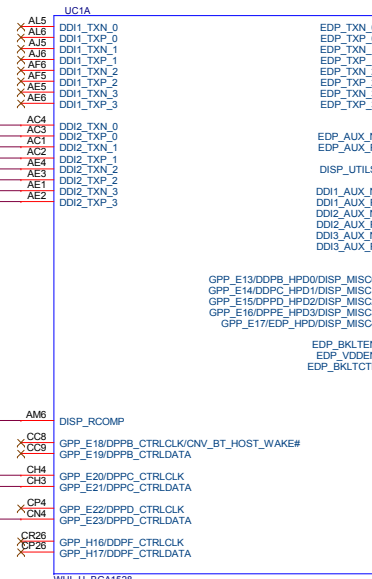


HDMI (Port 2)

<29,30> CPU_DP2_CTRL_CLK
<29,30> CPU_DP2_CTRL_DATA

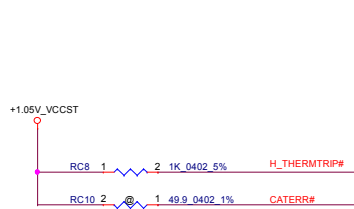
<28> TS_I2C_RST#

EDP_COMP



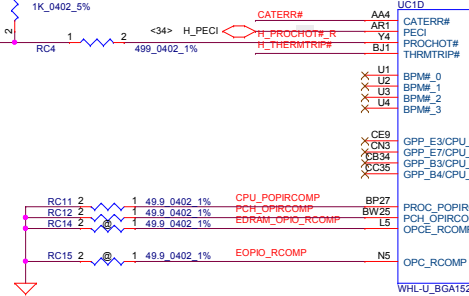
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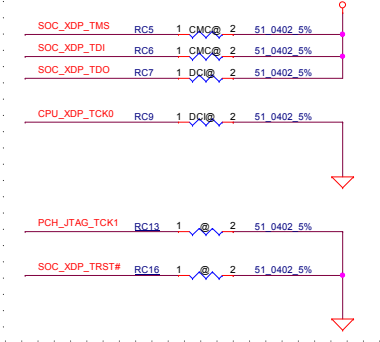
<34> H_PROCHOT#

If routed MS, PECl requires 18 mils spacing to other signals



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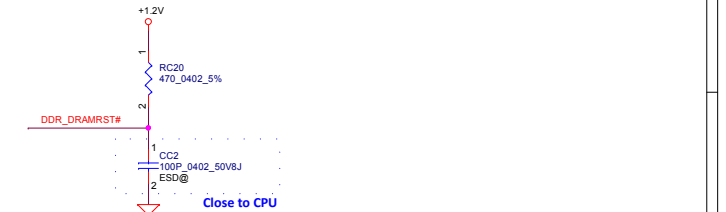
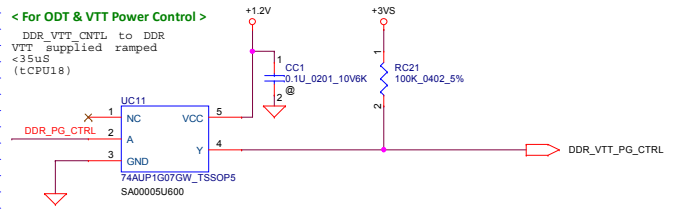
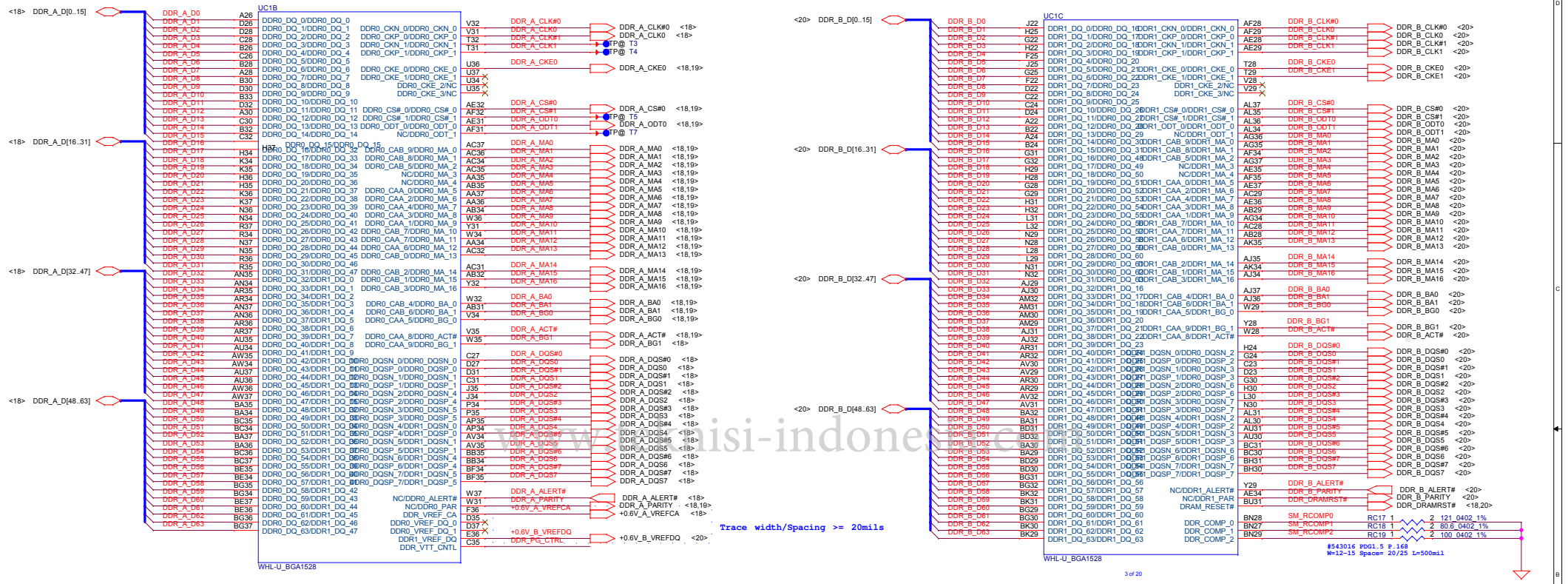
< PU/PD for CMC Debug >

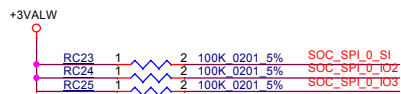


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								WHL-U(1/12)DDI.EDP.MISC.CMC			
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								Rev 0.A			

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Interleaved Memory





Note: The internal pull-up is disabled when RSMRST# is asserted (during reset) and only enabled after RSMRST# de-assertion

SML1ALERT#/
PCHHOT#/GPP_B23

- If USB 3.1 Port 1 is used for 4-wire DCI.OOB (BSSB), and alternate functionality is also used on the pin, pull up to V3.3S with >100K resistor to avoid noise.
- If USB 3.1 Port 1 is used for DCI.OOB (BSSB) 4-wire BSSB, and NO alternate functionality is used, leave float.
- If DCI.OOB (BSSB) 2+2 functionality is used, pull up to V3.3S with a 4.7K resistor]

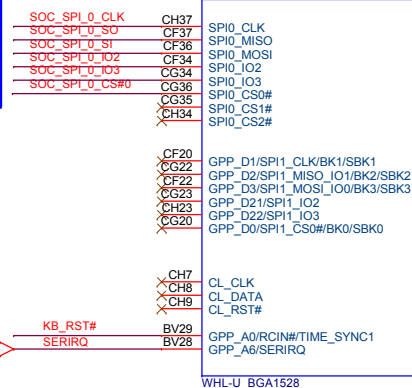
SML0ALERT# (Internal Pull Down):

eSPI or LPC

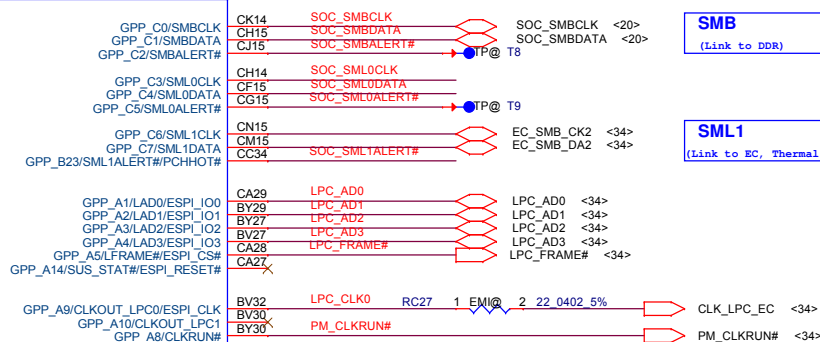
0 = LPC is selected for EC ==> Default

1 = eSPI is selected for EC

SPI ROM

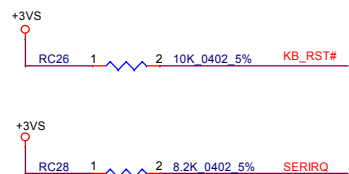


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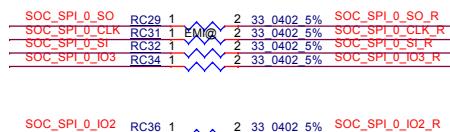


SMB
(Link to DDR)

SML1
(Link to EC, Thermal Sensor)



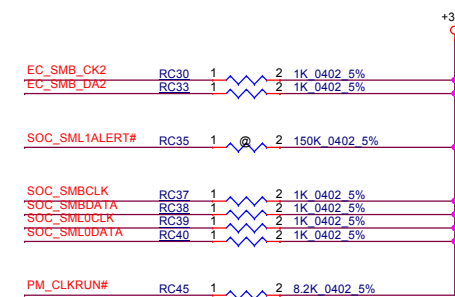
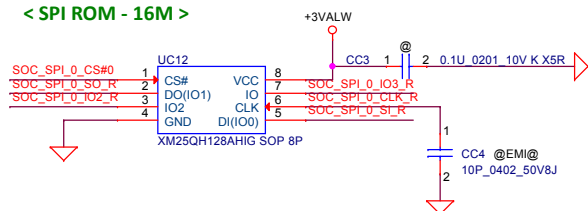
close to SPI ROM



From SOC

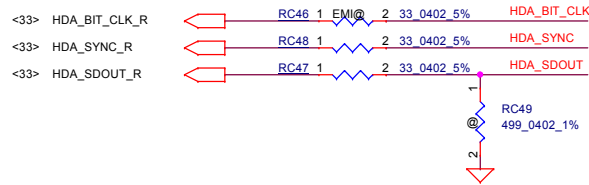
From EC

< SPI ROM - 16M >

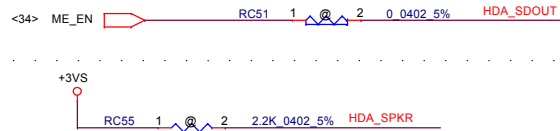


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< HD AUDIO >



< To Enable ME Override >



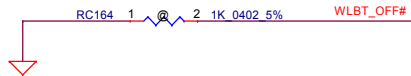
SPKR (Internal Pull Down):

TOP Swap Override

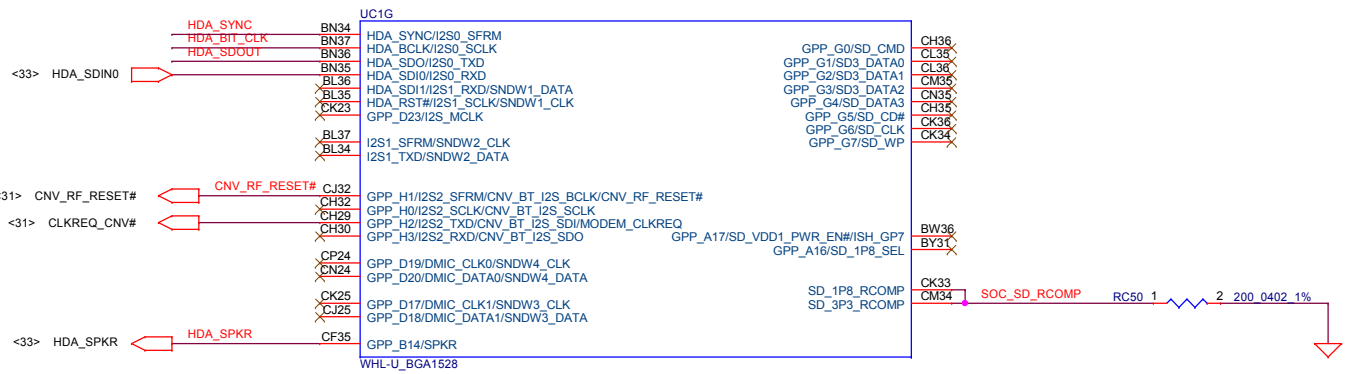
0 = Disable TOP Swap mode. ==> Default

1 = Enable TOP Swap Mode.

Follow Jefferson Peak schematic check list.

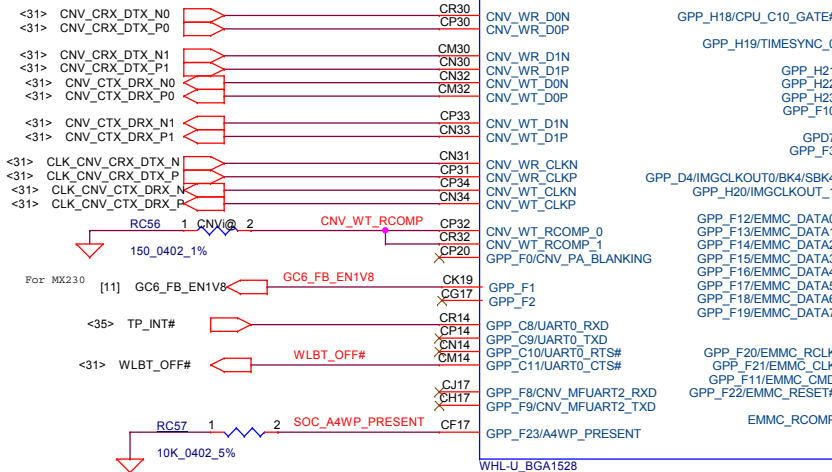


TO DGPU SOC_GPIO_C10 RC59 1 2 0.0402 5% GPU_EVENT# [24]



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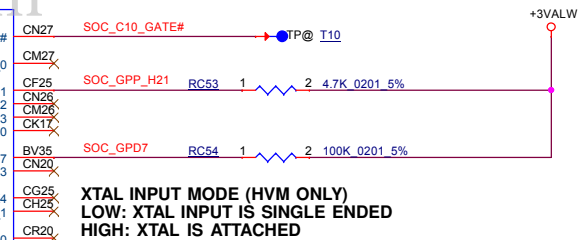


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GPP_H21 XTAL frequency select.

0: 38.4 / 19.2 MHz

1: 24MHz XTAL select.



XTAL INPUT MODE (HVM ONLY)
LOW: XTAL INPUT IS SINGLE ENDED
HIGH: XTAL IS ATTACHED

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GSPI0_MOSI (Internal Pull Down):

No Reboot

0 = Disable No Reboot mode. ==> Default

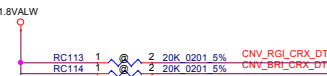
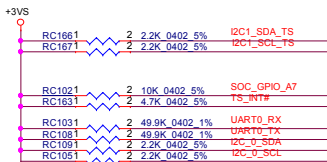
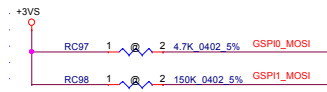
1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is used when running ITP/XDP.

GSPI1_MOSI (Internal Pull Down):

Boot BIOS Strap Bit

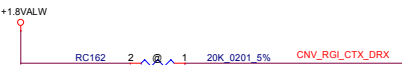
0 = SPI Mode ==> Default

1 = LPC Mode



Place close to PCH

for RMT test

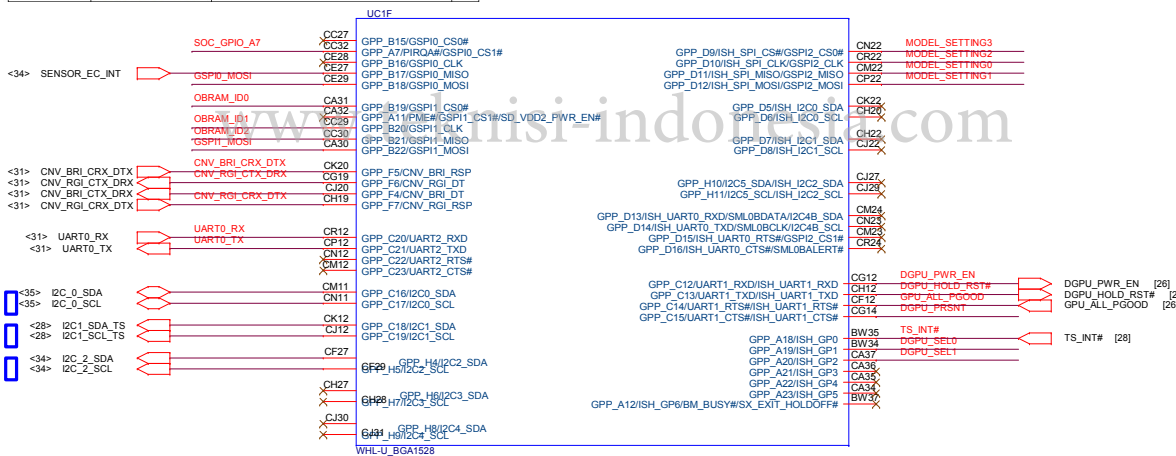


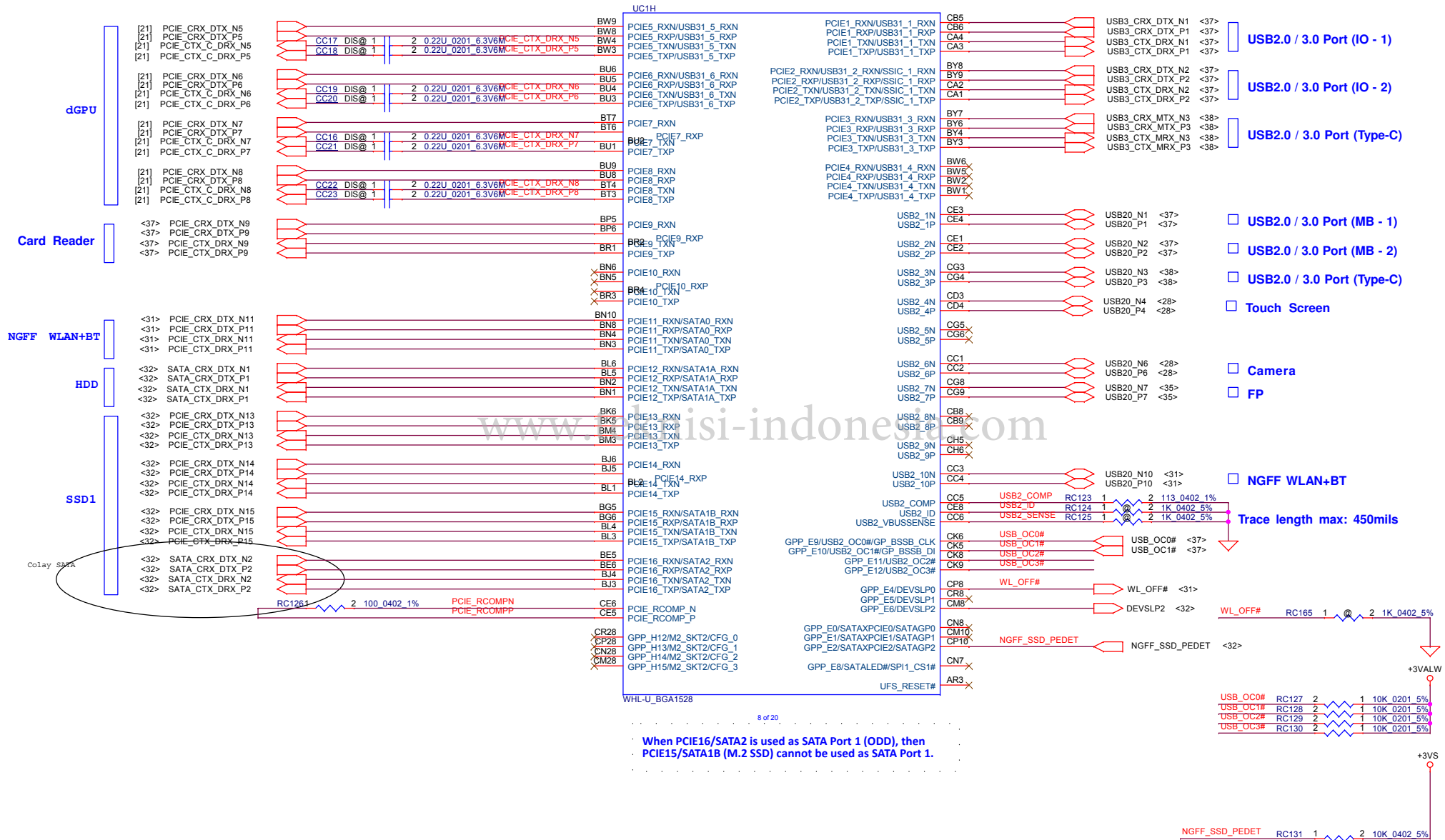
Capacity	Description	X76	PART NUMBER (R 1)
4GB	WITHOUT ON-BOARD RAM	NO_MD@	N/A
	HYNIX 2666MHz (H5AN8G6NCJR-VKC) S340	X7680438L81	SA0000BMN00
	HYNIX 2666MHz (H5AN8G6NCJR-VKC) C340	X7680538LA1	
	MICRON 2666MHz (MT40A512M16LY-075:E) S340	X7680438L82	SA0000ARD20
	MICRON 2666MHz (MT40A512M16LY-075:E) C340	X7680538LA2	
	SAMSUNG 2666MHz (K4A8G165WC-BCTD) S340	X7680438L83	SA0000B6F00
	SAMSUNG 2666MHz (K4A8G165WC-BCTD) C340	X7680538LA3	
	N/A	N/A	N/A

Capacity	Description	GPP_B19 OBRAM_ID0	GPP_B20 OBRAM_ID1	GPP_B21 OBRAM_ID2
4GB	WITHOUT ON-BOARD RAM	0	0	0
	SAMSUNG 2666MHz (K4A8G165WC-BCTD)	0	0	1
	HYNIX 2666MHz (H5AN8G6NCJR-VKC)	0	1	0
	MICRON 2666MHz (MT40A512M16LY-075:E)	0	1	1
	N/A	1	0	0
	N/A	1	0	1
	N/A	1	1	0
	N/A	1	1	1

Table 1-26 Miscellaneous Signals on the Processor Checklist:

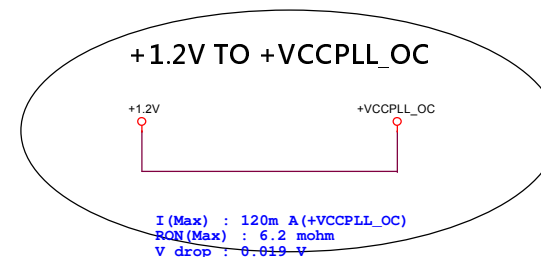
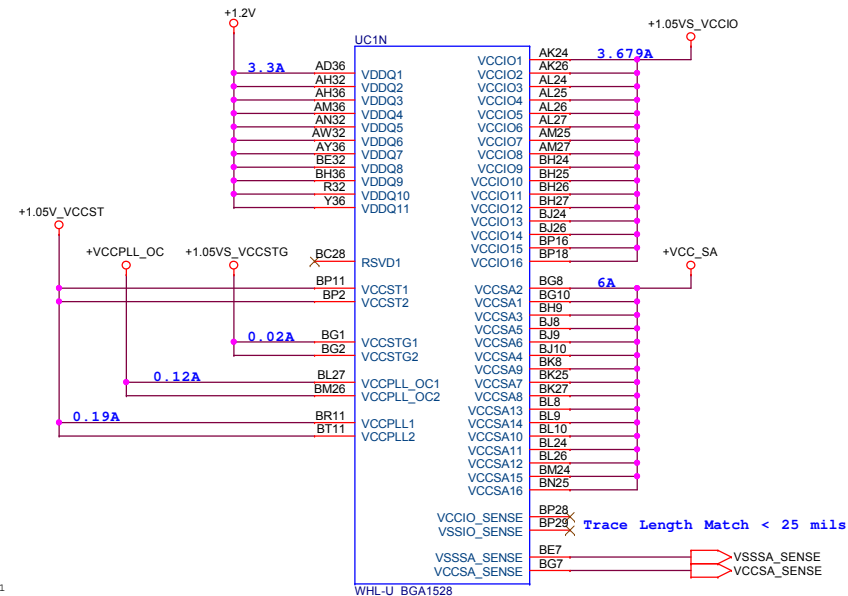
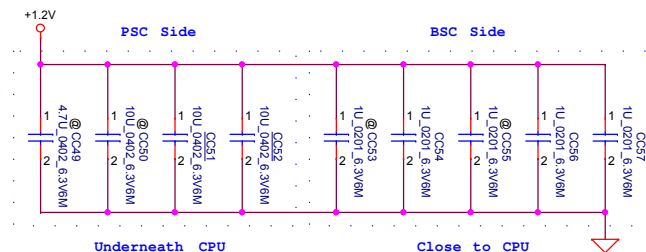
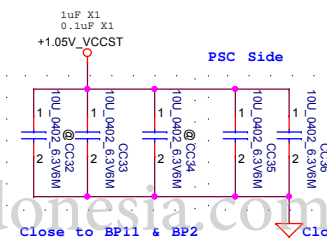
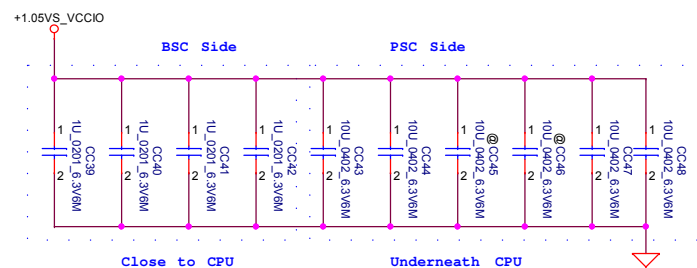
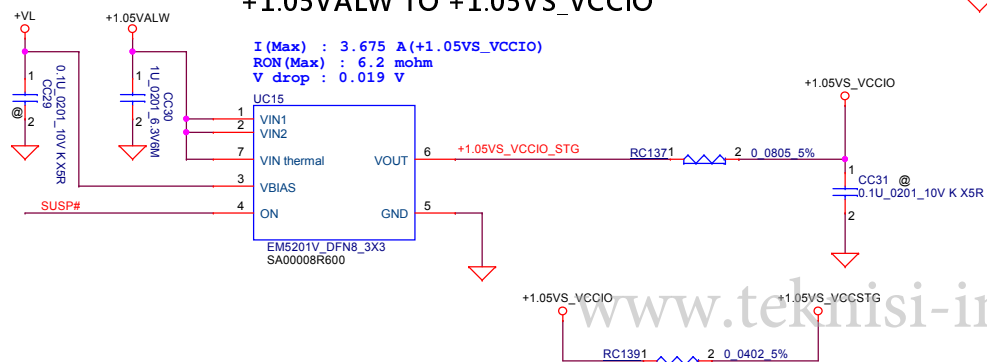
Pin Name	System Pull-up / Pull-down	Schematics Notes	
RCIN# / GPP_A0	Pull-up to V3.35 with 10 KΩ resistor.	Driven by discrete glue logic or I/O which act as keyboard controller to generate INIT# to the processor.	
PROCPWRGD		This signal is indication of PROCPWRGOOD.	
PIRQA# / GPP_A7	Pull-up to V3.35 with 8.2 KΩ -> 10 KΩ resistor.		



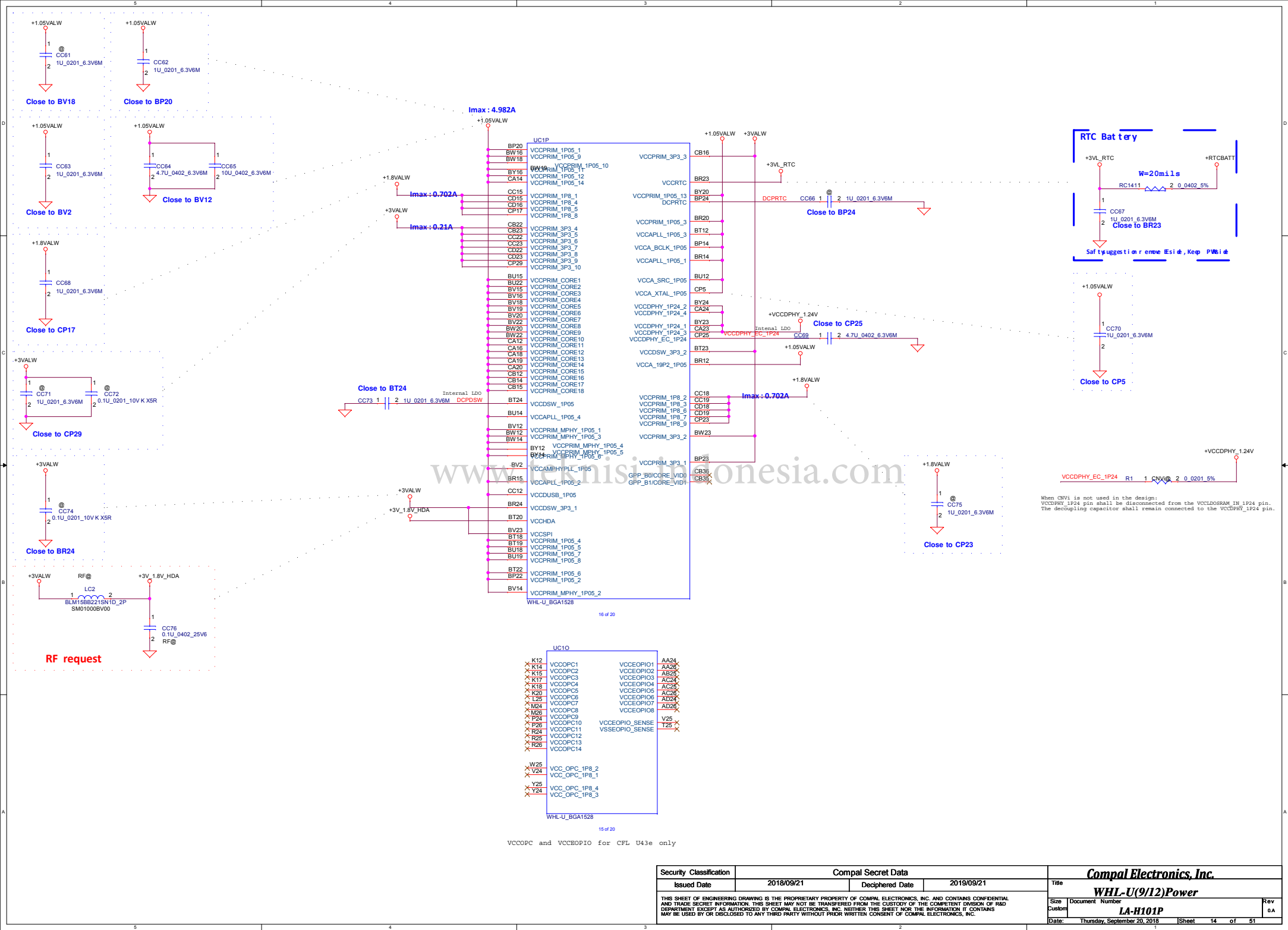


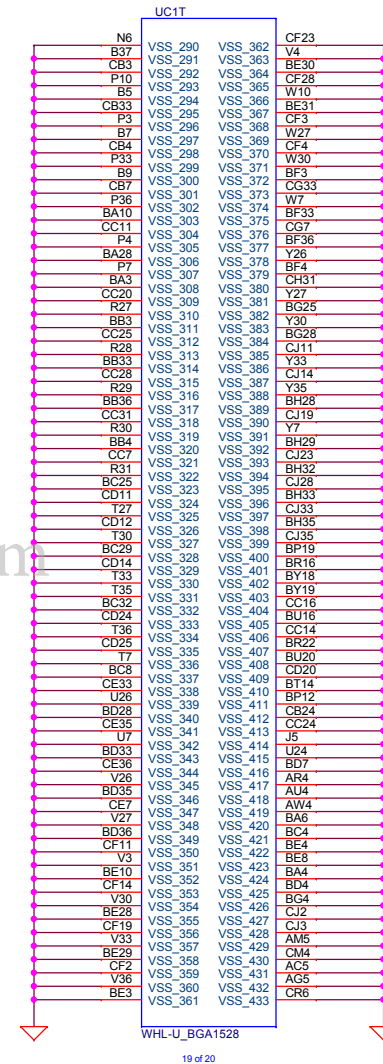
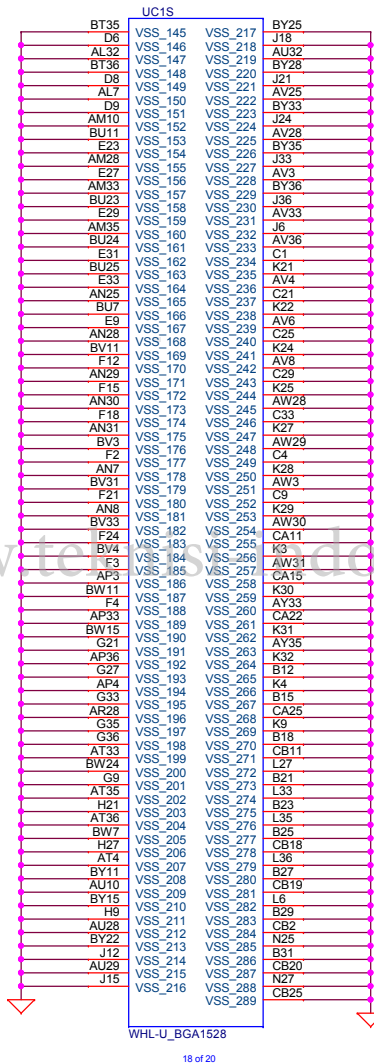
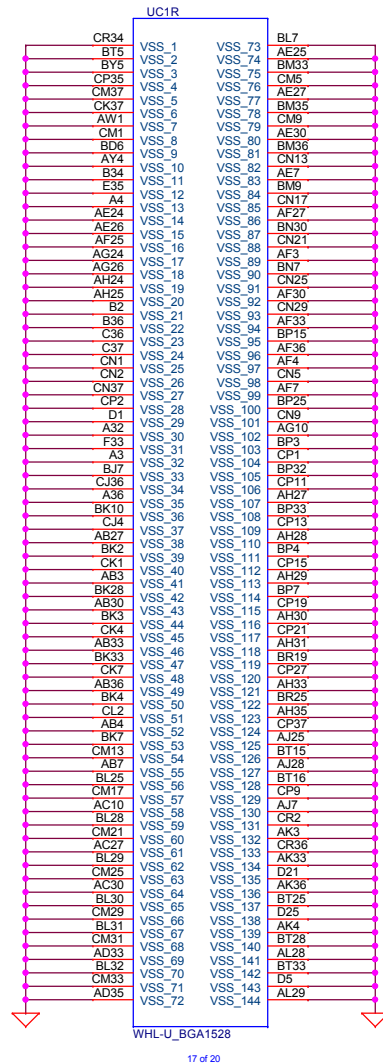
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+1.05VALW TO +1.05VS VCCIO

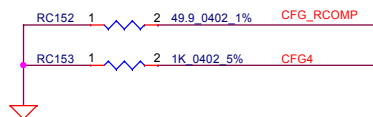


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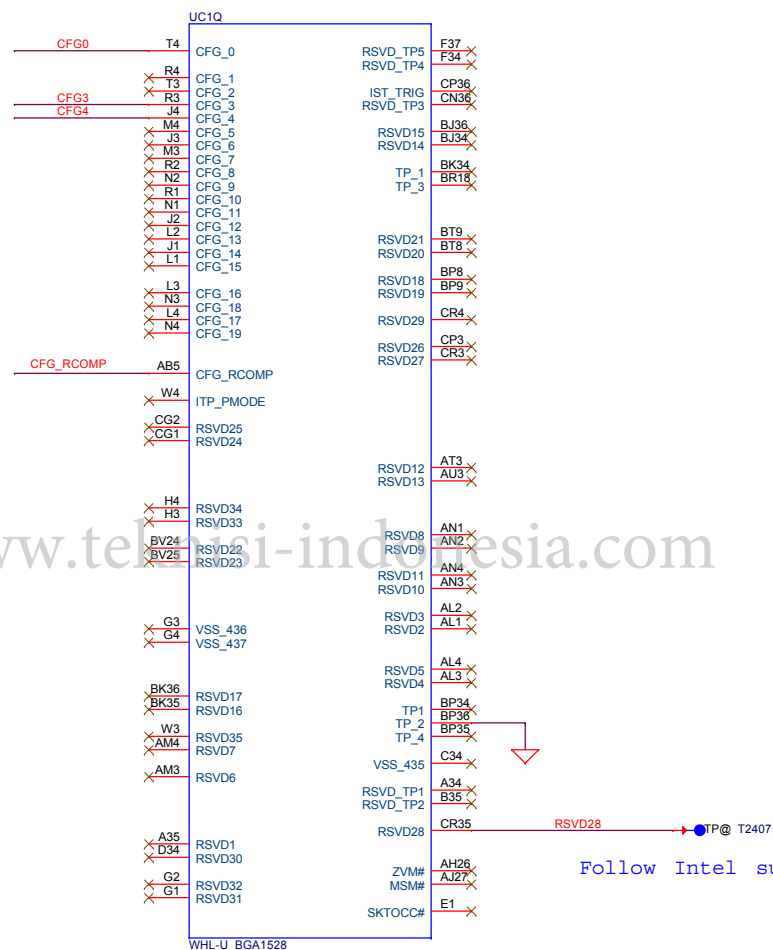




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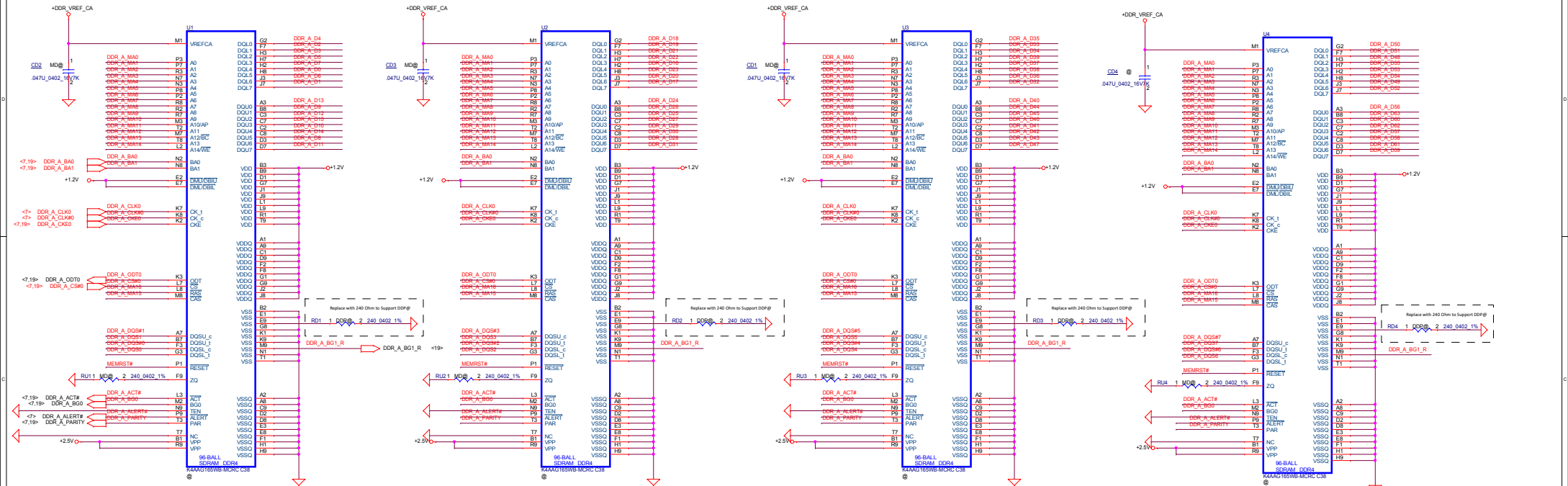


DFX Privacy Strap	
CFG3	<p>1 : Disabled; Set DFX disable bit in debug interface MSR</p> <p>0 : Enabled; Set DFX enable bit in debug interface MSR</p>
Display Port Presence Strap	
CFG4	<p>1 : Disabled; No Physical Display Port at tached o E mbedded Dsplay port</p> <p>0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p>

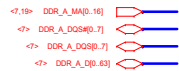


Follow Intel suggetion reserve TP

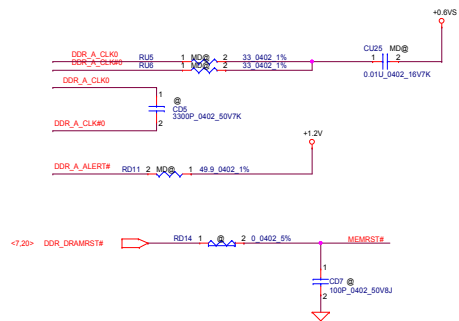
Interleaved Memory



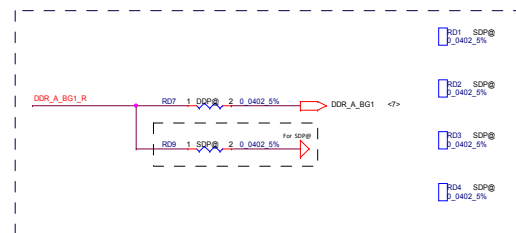
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CLOCK TERMINATION

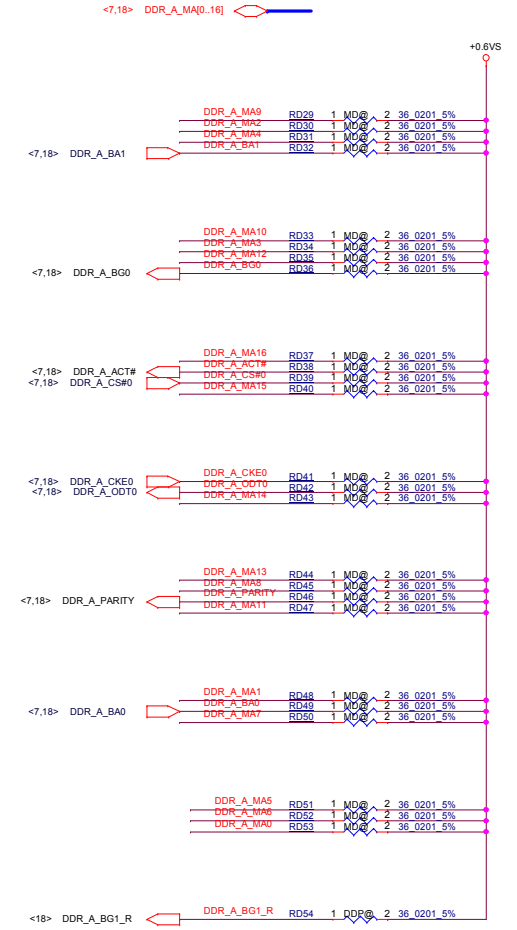
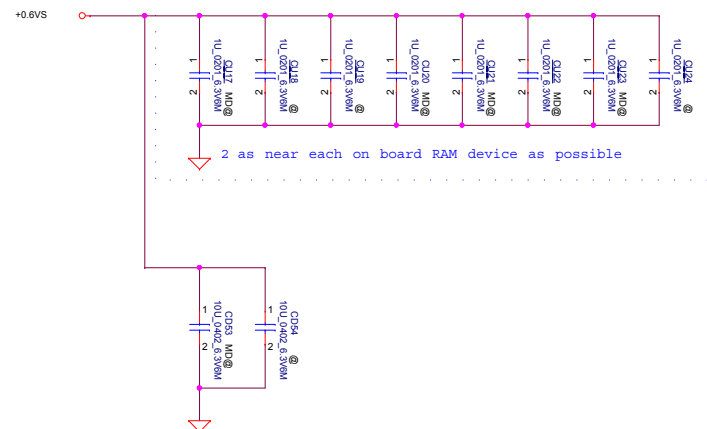
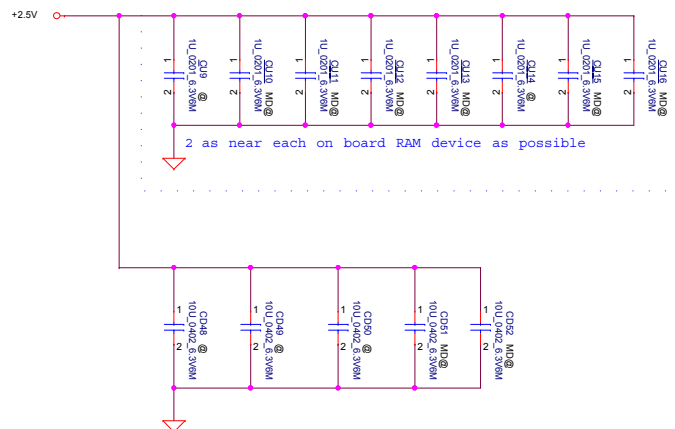
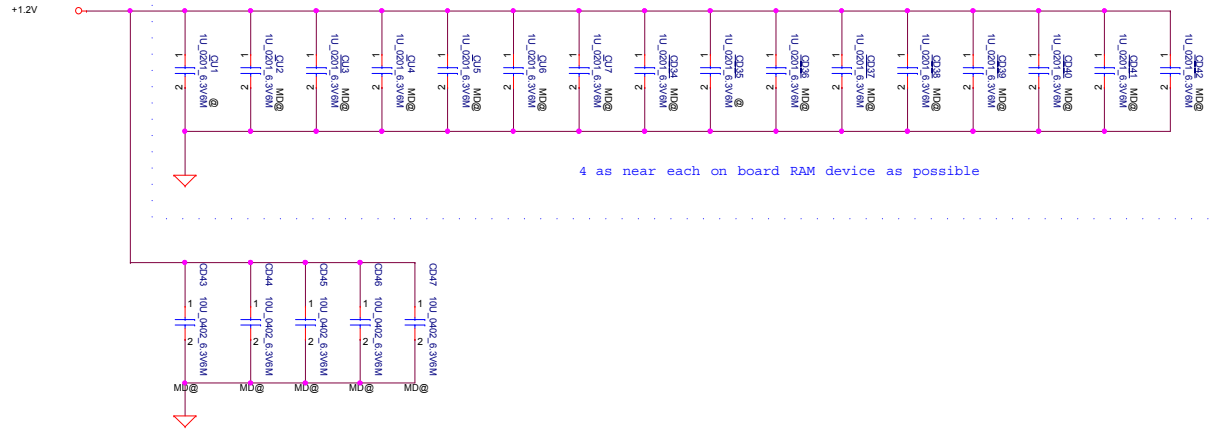


Co-layer for SDP / DDP Memory DIE



On Board RAM - Data Mapping

U4	D0	U2	D0	U3	D0	U1	D0
DQL0	D13	DQL0	D29	DQL0	D43	DQL0	D60
DQL1	D12	DQL1	D25	DQL1	D40	DQL1	D61
DQL2	D11	DQL2	D27	DQL2	D42	DQL2	D62
DQL3	D8	DQL3	D24	DQL3	D41	DQL3	D57
DQL4	D10	DQL4	D30	DQL4	D47	DQL4	D58
DQL5	D9	DQL5	D28	DQL5	D45	DQL5	D56
DQL6	D14	DQL6	D31	DQL6	D46	DQL6	D59
DQL7	D15	DQL7	D26	DQL7	D44	DQL7	D63
DQU0	D6	DQU0	D22	DQU0	D38	DQU0	D50
DQU1	D1	DQU1	D17	DQU1	D37	DQU1	D52
DQU2	D7	DQU2	D23	DQU2	D35	DQU2	D51
DQU3	D5	DQU3	D20	DQU3	D32	DQU3	D48
DQU4	D3	DQU4	D19	DQU4	D33	DQU4	D54
DQU5	D4	DQU5	D16	DQU5	D36	DQU5	D53
DQU6	D2	DQU6	D18	DQU6	D39	DQU6	D55
DQU7	D0	DQU7	D21	DQU7	D34	DQU7	D49

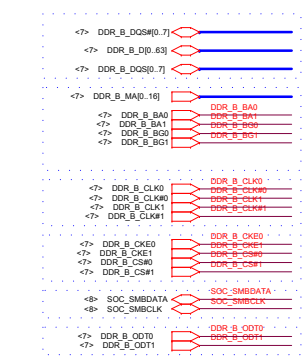


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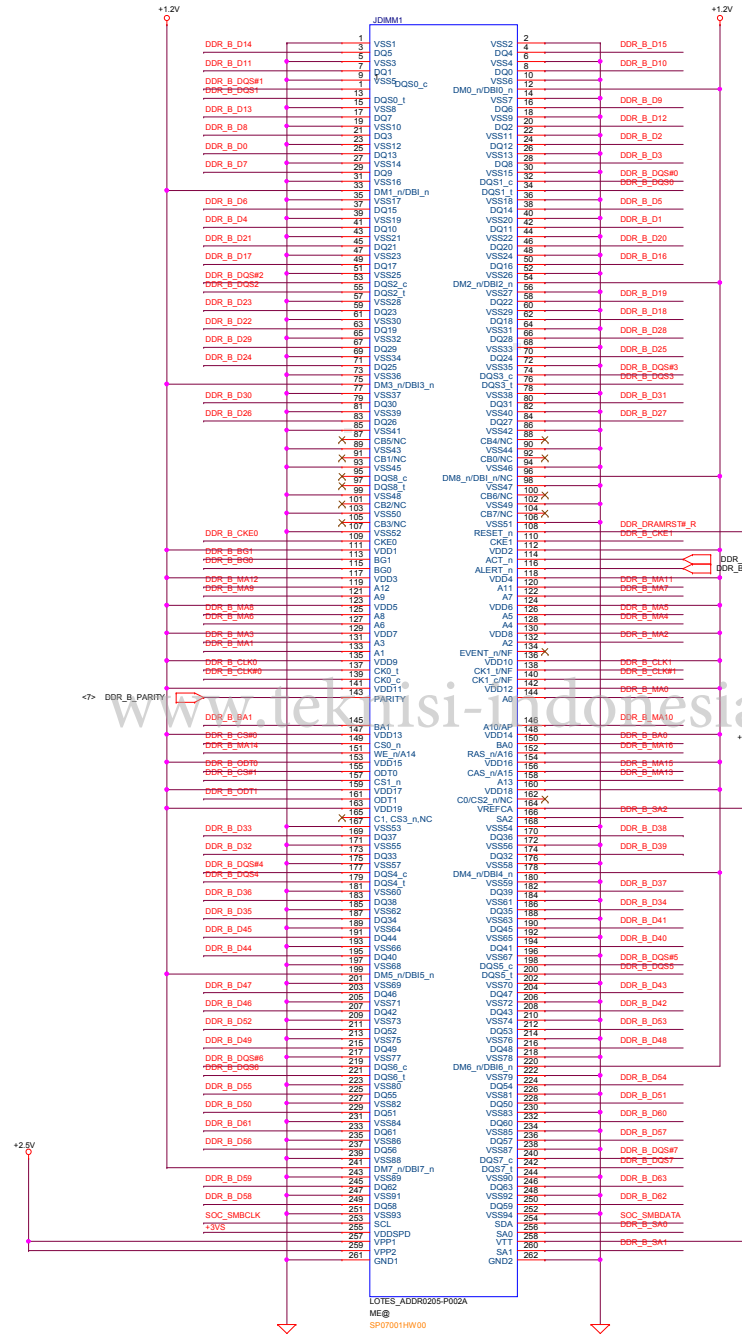
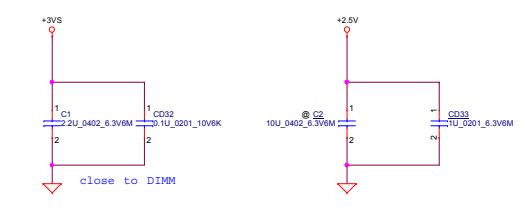
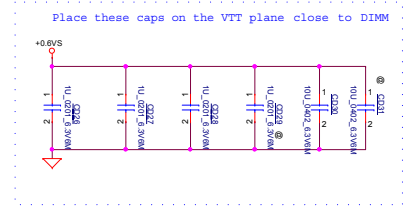
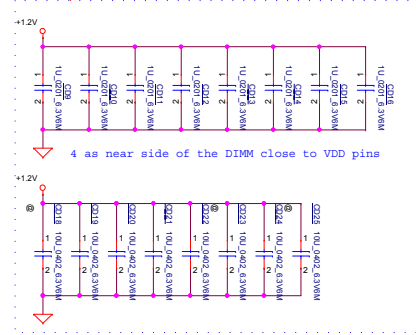
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LA-H101P

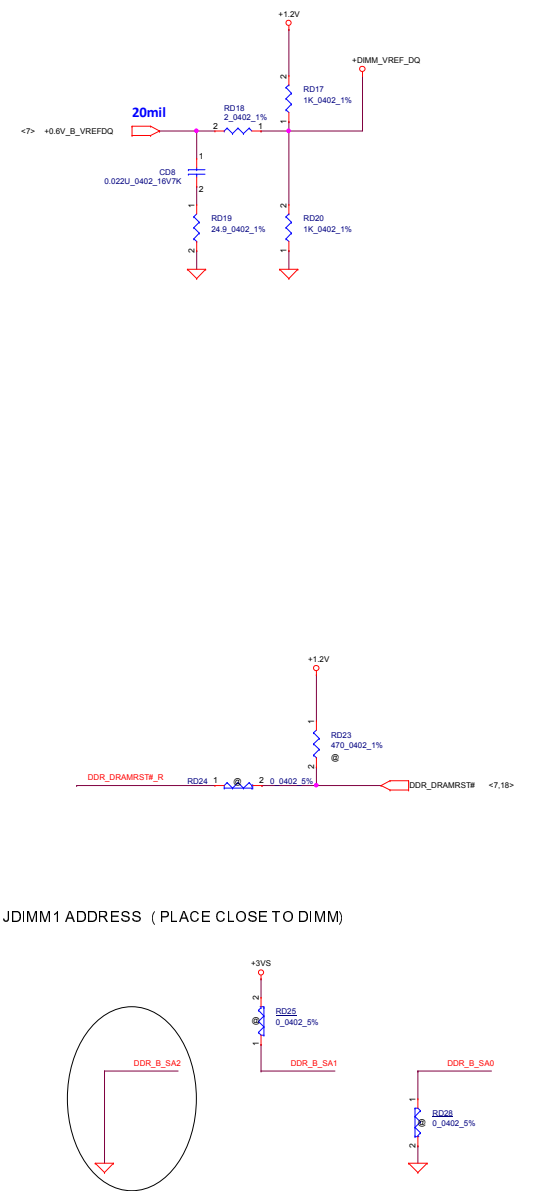


Layout Note:
Place near JDIMM1

Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket



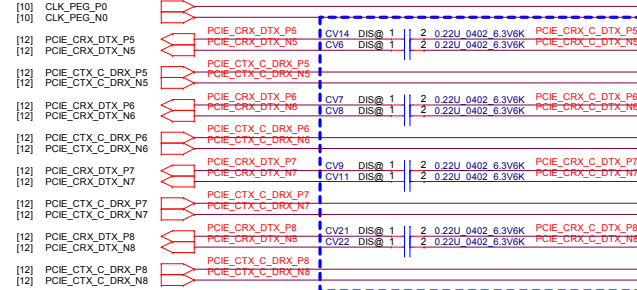
Standard Type
2-3A to 1 DIMMs/channel



JDIMM1 ADDRESS (PLACE CLOSE TO DIMM)

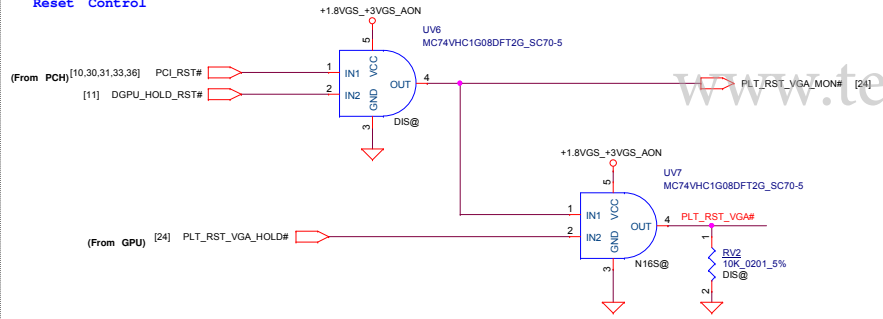
PCIE CLK

PCIE X4 Bus

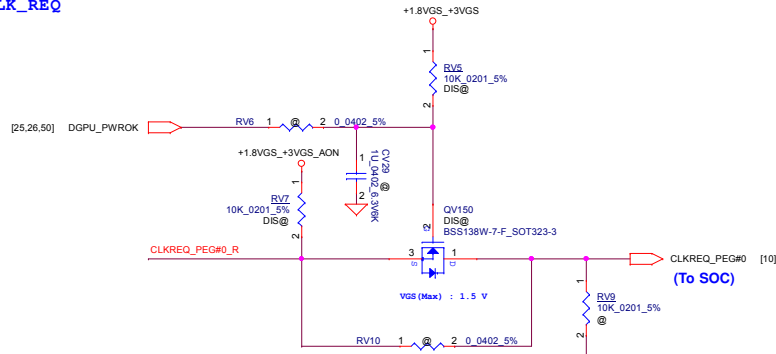


Near UV1

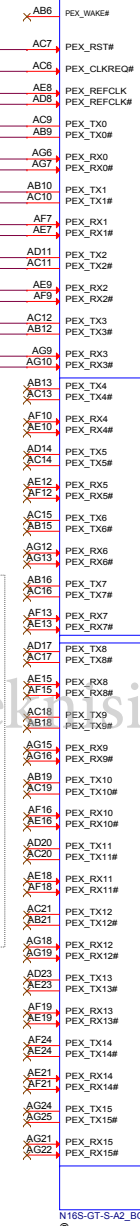
Reset Control



CLK_REQ



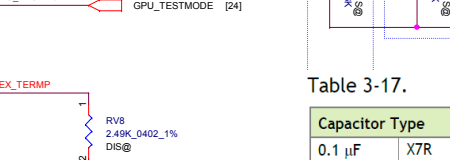
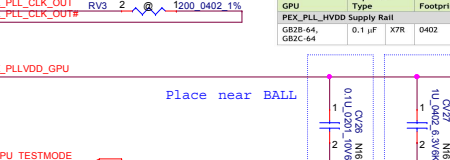
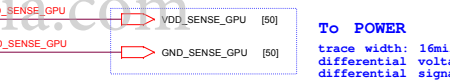
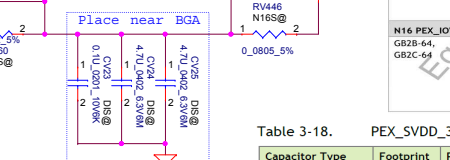
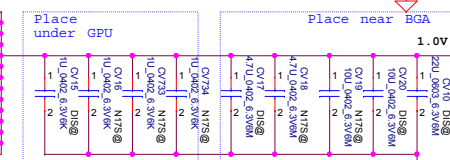
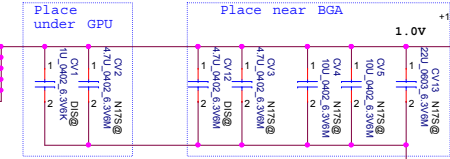
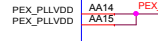
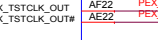
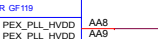
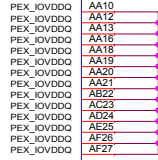
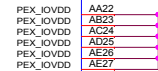
UV1A COMMON



NC FOR GM108

NC FOR GF117/GK208/GM108

N16S-GT-S-A2_BGA595



GPU Package Type	Capacitor Type	Footprint	Population	Location
GB2B-64	1.0 μ F	X65	0402	1 Under GPU
GB2C-64	4.7 μ F	X65	0603	1 Near GPU
	10 μ F	X5R	0805	1 Midway between GPU and Power Supply
	22 μ F	X5R	0805	1 Midway between GPU and Power Supply

Table 6. PEX Core and IO Supply Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population	Location
N16 PEX_IOVDD (N17 PEX_VDD) Supply Rail				
GB2B-64	1.0 μ F	X65	0402	1 Under GPU
GB2C-64	4.7 μ F	X65	0603	1 Under GPU
	4.7 μ F	X65	0603	2 Near GPU
	10 μ F	X65	0805	1 Midway between GPU and Power Supply
	22 μ F	X65	0805	0 2 Midway between GPU and Power Supply
N16 PEX_IOVDD (N17 PEX_HVDD) Supply Rail				
GB2B-64	1.0 μ F	X65	0402	1 Under GPU
GB2C-64	4.7 μ F	X65	0603	1 Near GPU
	10 μ F	X65	0805LP	1 2 Midway between GPU and Power Supply
	22 μ F	X65	0805LP	1 1 Midway between GPU and Power Supply

Table 3-18. PEX_SVDD_3V3 and PEX_PLL_HVDD Decoupling

Capacitor Type	Footprint	Population	Location
0.1 μ F	X7R	0402	1 Near GPU
4.7 μ F	X5R	0603	2 Near GPU

To POWER
trace width: 16mils
differential voltage sensing.
differential signal routing.

Table 7. PEX PLLs Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population	Location
PEX_PLLVDD Supply Rail				
GB2B-64	0.1 μ F	X7R	0402	1 N/A Under GPU
	1.0 μ F	X5R	0603	1 N/A Near GPU
	4.7 μ F	X5R	0805	1 N/A Near GPU
PEX_SVDD_3V3 Supply Rail				
GB2B-64	4.7 μ F	X5R	0603	2 N/A Near GPU
GPU	Capacitor Type	Footprint	Population	Location
PEX_PLL_HVDD Supply Rail				
GB2B-64	0.1 μ F	X7R	0402	1 1 Near GPU

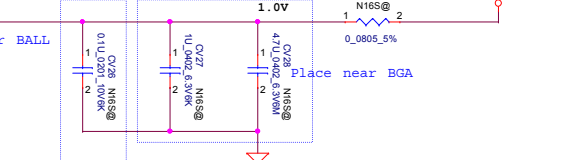


Table 3-17. PEX_PLLVDD Decoupling

Capacitor Type	Footprint	Population	Location
0.1 μ F	X7R	0402	1 Under GPU
1.0 μ F	X5R	0603	1 Near GPU
4.7 μ F	X5R	0805	1 Near GPU

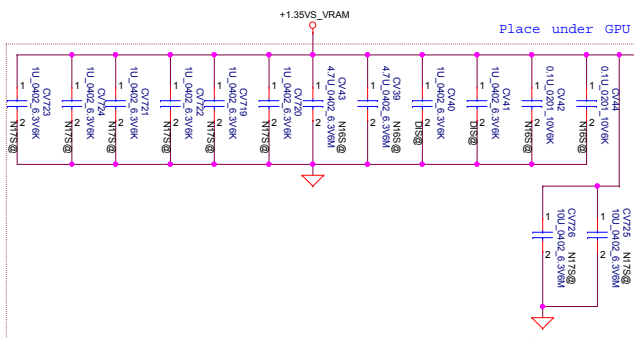
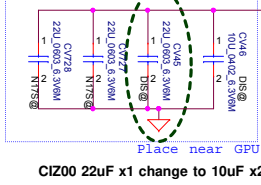
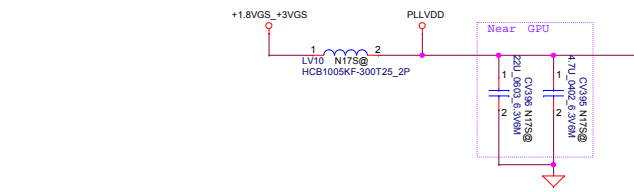


Table 4. Frame Buffer Core and IO Decoupling and Filtering

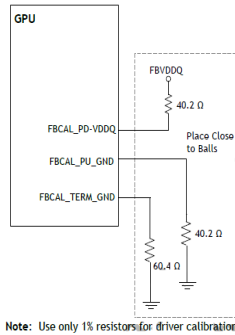
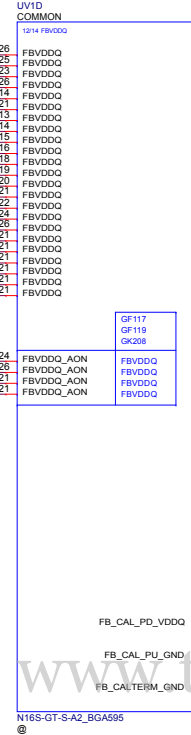
GPU	Capacitor Type	Footprint	Population	N16	N17	Location
FBVDD/Q Supply Rail for GDDR5						
GB2B-64, GB2C-64	0.1 μ F	X7R	0402	2	0	Under GPU
	1 μ F	X7R	0603	2	8	Under GPU
	4.7 μ F	X65	0603	2	0	Under GPU
	10 μ F	X65	0603	0	2	Under GPU
	10 μ F	X65	0603	1	1	Near GPU
	22 μ F	X65	0603W	1	3	Near GPU



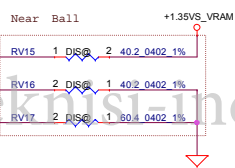
GPU Package Type	Capacitor Type	Footprint	Population		Location
GB2B-64/ GB2-64 GDDR5	0.1 μ F	X7R	0402	2	Under GPU
	1 μ F	X7R	0603	2	Under GPU
	4.7 μ F	X6S	0603	2	Under GPU
	10 μ F	X5R	0805	1	Near GPU
	22 μ F	X5R	0805	1	Near GPU



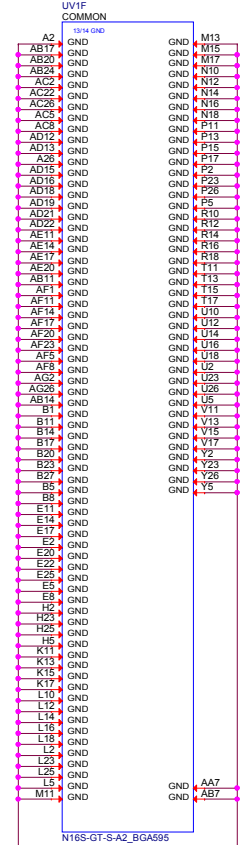
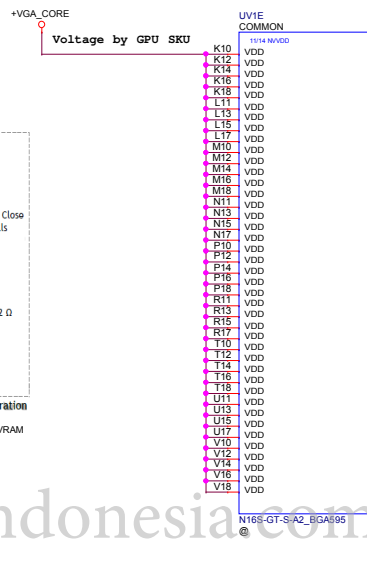
NC (N17: GPCPLL_AVDD) Supply Rail						
GB2C-64	0.1 μ F	X7R	0402	N/A	1	Under GPU
	4.7 μ F	X6S	0603	N/A	1	Near GPU
	22 μ F	X6S	0805	N/A	1	Near GPU
	Bead Type					
	L=30 Ω (ESR=0.010 Ω)	0603	N/A	1	Near GPU	



Note: Use only 1% resistors for driver calibration



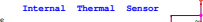
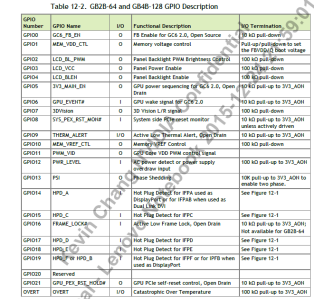
GPU_Decoupling CAPs @ Power Page



GPU Package	Rail	Capacitor Type		Footprint		Population	Location
GB2-64	3V3_MAIN	0.1 μ F	X6S	0402	2	2	Under GPU
GB2B-64		1 μ F	X5R	0603	1	1	Near GPU
GB4B-128		4.7 μ F	X5R	0603	1	1	Near GPU
GB3B-256							
GB2-64	3V3_AQN	0.1 μ F	X6S	0402	1	1	Under GPU
GB2B-64		1 μ F	X5R	0603	1	1	Near GPU
GB4B-128		4.7 μ F	X5R	0603	1	1	Near GPU
GB3B-256							

Note: This table is for non-SLI mode. For SLI mode, please refer to the MIO Decoupling table.

Note: This table is for non-SLI mode. For SLI mode, please refer to the MIO Decoupling table.



al Thermal Sensor

[Link to PCH SML1](#)

NV Suggest

CMR150 (S0)	Item	Part No.	Part No.
	Item	N160-G0M0120120	N160-G0M0120120
Device ID	ID#174E		
Package	GB48-128/GB28-64	GB48-128/GB28-64	GB48-128/GB28-64
ROM_S1	Refer to N160_XM8_Storage table	Refer to N160_XM8_Storage table	
ROM_S2	0x0000, 4.599MHz pull-up	0x0000, 4.599MHz pull-up	
ROM_S3L0	0x0000, 4.599MHz pull-down	0x0000, 4.599MHz pull-down	
Strap0	Reserved Keep pull-up on SV3_A0N and pull-down footprints and SV3_C0(N) pull-up	Reserved Keep pull-up on SV3_A0N and pull-down footprints and SV3_C0(N) pull-up	
Strap2	Reserved (Keep pull-up and pull-down footprints and leave them not stuffed by default)	Reserved (Keep pull-up and pull-down footprints and leave them not stuffed by default)	
Strap3	Reserved (Keep pull-up and pull-down footprints and leave them not stuffed by default)	Reserved (Keep pull-up and pull-down footprints and leave them not stuffed by default)	
Strap4	Reserved (Keep pull-up and pull-down footprints and leave them not stuffed by default)	Reserved (Keep pull-up and pull-down footprints and leave them not stuffed by default)	
Open_VDD_S01	0.5V	0.5V	
NVDDIO Stand-By Voltage	0.9V	0.9V	

Table 5.5 SORx_EXPOSED Strap Enablement for Down DesignsTable 5.6 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins (note 1)			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SWB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	0
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	H	L	0	1	0	1
H	H	H	0	1	1	0
H	H	H	0	1	1	1

Table 5. N17S-G0/G2 GDOR.
















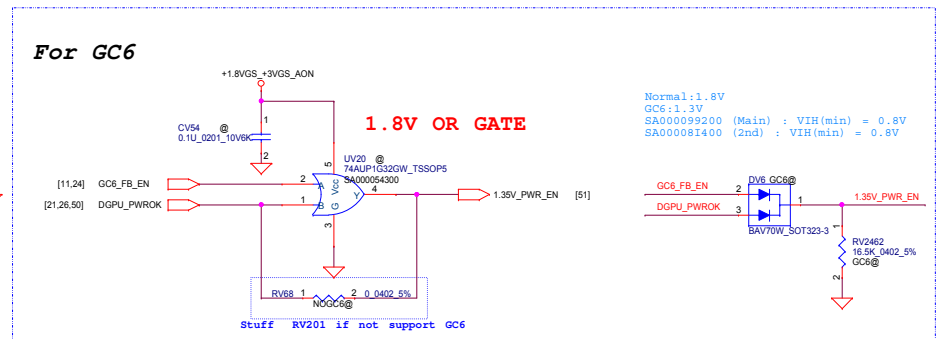
RAM_CFG	STRAP2	STRAP1	STRAP0	NOTE
0x3 (LML) M2G	 N17_M0G@ 100K_0402_5%	 D001 N17_M0G@ 100K_0402_5%	 D003 N17_M0G@ 100K_0402_5%	
0xA (LML) H2G	 N17_M0G@ 100K_0402_5%	 D001 N17_M0G@ 100K_0402_5%	 D003 N17_M0G@ 100K_0402_5%	

Table 5.3 RAMCFG

Strap Pins see Note			RAACE6 Setting Number	
STRAP1	STRAP2	STRAP3	(see Memory RVL for memory configs corresponding to these numbers)	
L	L	L	0	(0x0000)
L	L	R	1	(0x0001)
L	H	L	2	(0x0002)
L	H	R	3	(0x0003)
M	L	M	4	(0x0004)
M	L	H	5	(0x0005)
M	H	L	6	(0x0006)
M	H	R	7	(0x0007)
L	L	M	8	(0x0008)
L	M	L	9	(0x0009)
L	M	R	10	(0x000A)

4. N175-G1 GDORS Recommendation

RAN_CFG	STRA2	STRA1	STRA0
0x00 (LL1) S2G	 0x000 S	 0x000 S	 0x000 S
0x01 (LL8)			
0x02 (LL1)			
0x03 (LL8B)			
0x04 (RL1) M2G	 0x000 M	 0x000 M	 0x000 M
0x05 (RL8B) S2G	 0x000 S	 0x000 S	 0x004 S
0x06 (RL1)			
0x07 (RL8B)			
0x08 (LLM)			



The diagram illustrates the GPU interface for GDDR5 memory. It shows two signal lines, CKE1* and CKE0*, originating from the GPU. Each line is connected to a 10 kΩ pull-up resistor, which is then connected to the FBVDDQ pin of a GDDR5 memory chip. The GDDR5 chip is labeled as '1 chip in x32 mode' and 'Single Load'.

GPU Package	Rail	Capacitor Type	Footprint	Population	Location	
GB2-64/ GB28-64	FBx_PLL_AVDD and FB_DLL_AVDD Combined	0.1 μ F	X7R	2	Under GPU	
		22 μ F	X5R	1	Near GPU	
		Bead Type				
		30 Ω (ESR=0.010 Ω)	0603	1	Near GPU	

GPU	Capacitor Type	Footprint	Population		Location
			N16	N17	
FB PLL Supply Rail for GDDR5					
GB2B-64,	0.1 μ F	X402	2	4	Under GPU
GB2C-64	22 μ F	X65 0805	1	1	Near GPU
	Bead Type				
	30 Ω (03R-0.010 Ω)	0603	1	1	Near GPU

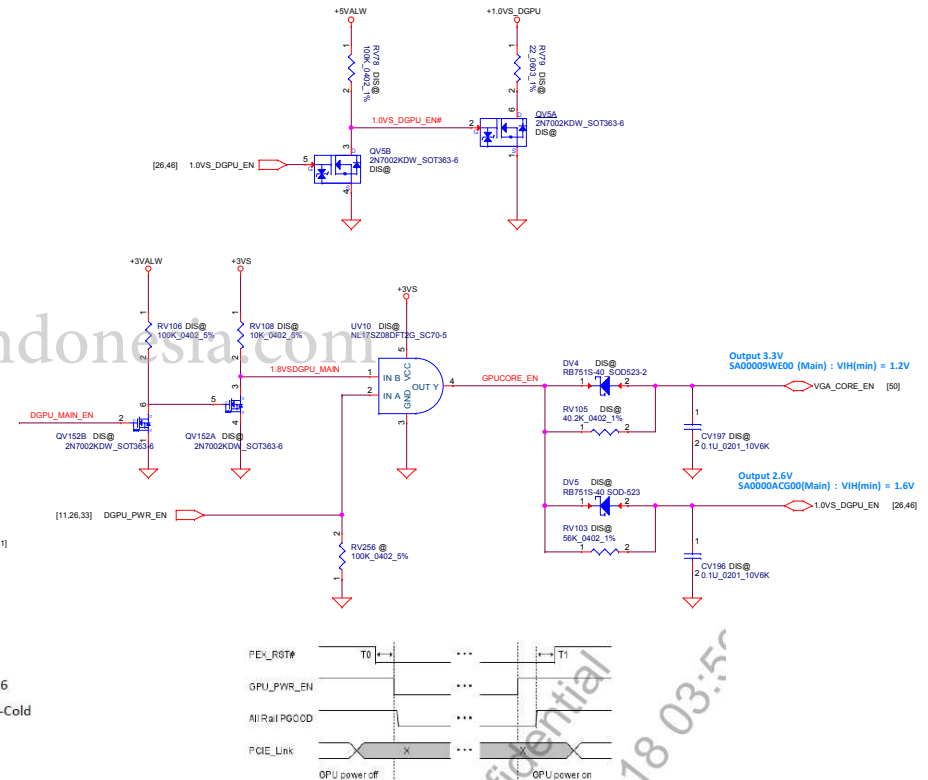
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Issued Date	2017/10/27	Deciphered Date	2019/04/09	Title	NV(5/5)-MEMORY FBA	
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Timing diagram showing the sequence of power-up events for various voltage rails. The rails are 1V8_AON, 1V8_MAIN, NVVDD, NVVDDS, PEX_VDD, and FBVDD/Q. The diagram illustrates the timing relationship between these rails, specifically highlighting the delay t_1 between NVVDD and NVVDDS. A note states: t_1 must not exceed 4ms.

The diagram shows the timing for the 1V8_MAIN power down sequence. The signals are: 1V8_AON, 1V8_MAIN, NVVD, NVVDS, PEX_VDD, and FBVDD/Q. 1V8_AON is high. 1V8_MAIN is high until a vertical blue line, then ramps down. NVVD and NVVDS are high until the blue line, then drop. PEX_VDD has a pulse before the blue line. FBVDD/Q is high until the blue line, then drops. A dashed line labeled 'D3-Colo' indicates a signal that drops at the blue line. A horizontal double-headed arrow at the bottom is labeled '1V8_MAIN (must be powered down)'. A 'GC6' label is at the top right.

1V8_MAIN must be powered down

	NVDD	GPU FBIO	FB Total ⁵	1.0V Total ¹	1.8V Total
	—	1.35V ⁴	1.35V ⁴	1.0V ⁴	1.8V ⁴
Product	(A)	(A)	(A)	(A)	(A)
N175-LG	15.4	2.5	5.0	0.1	0.2
N175-G1	30.0	3.0	5.6	0.1	0.3
N175-G0 ⁶	27.8	3.2	5.8	0.2	0.5
N175-G2 ⁶	28.6	3.2	5.8	0.2	0.5



Symbol	Description	Min	Max	Unit
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# de-assertion	0.1	5	ms

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Date:	Monday, October 22, 2018	Issued By:	26	c	88

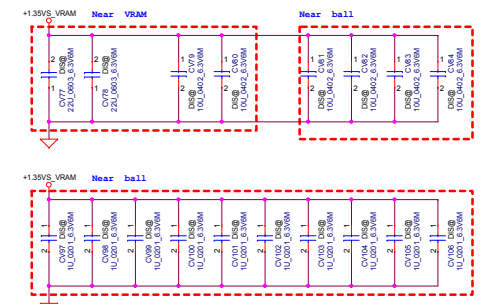
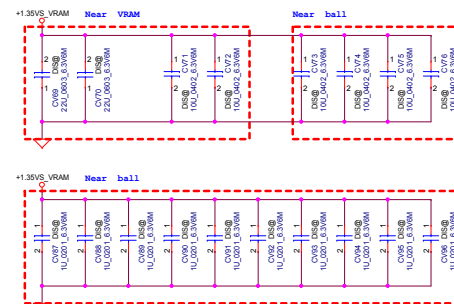
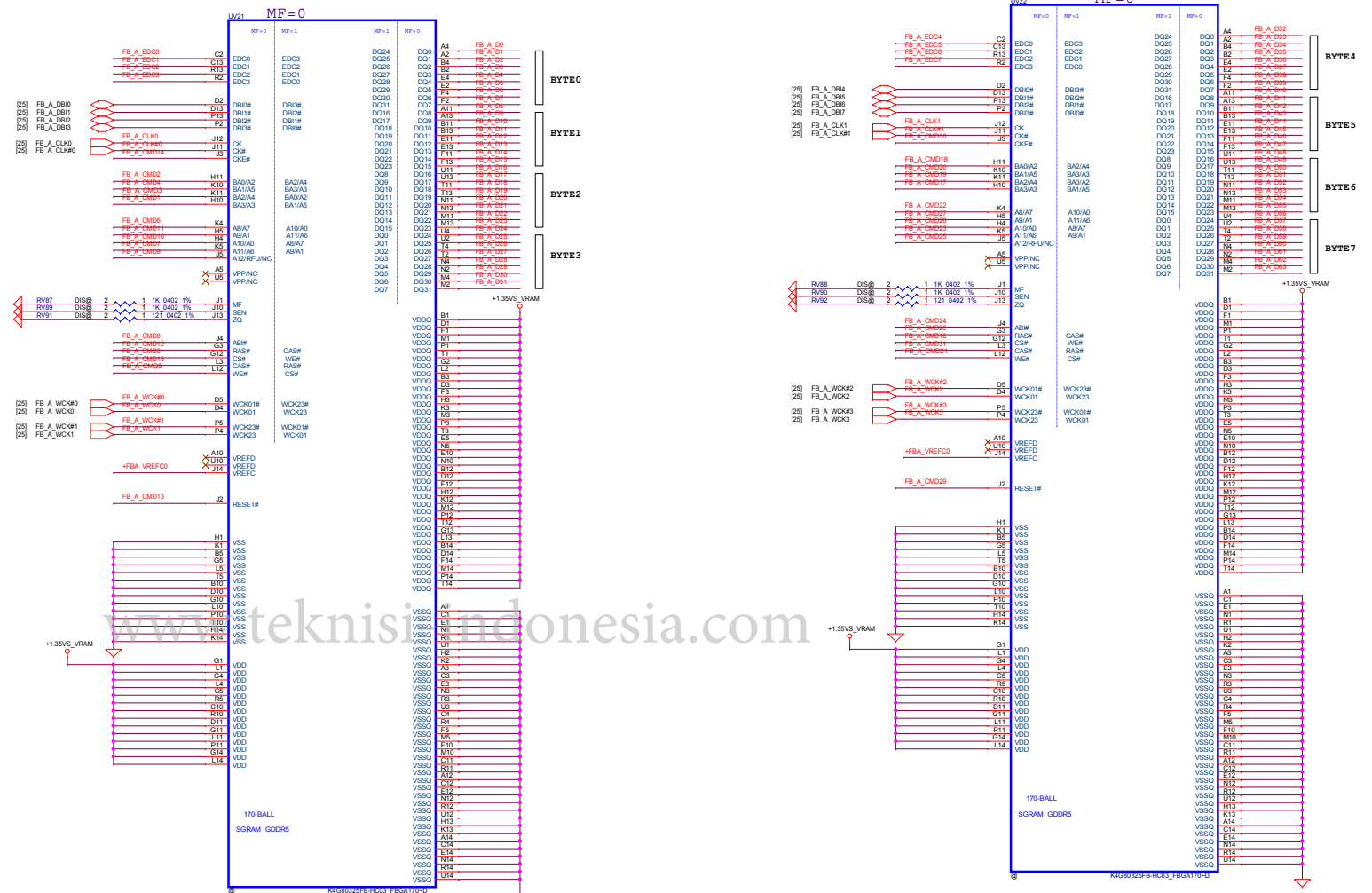
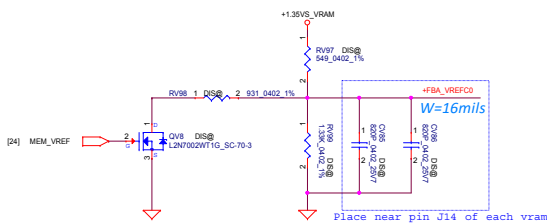
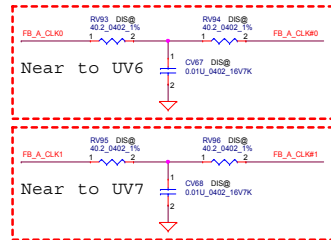
Table 7-4. GDDR5 Mode H Mapping

GB2-64, GB28-64, GB48-128		Channel 0 0.31	GB2-64, GB28-64, GB48-128	Channel 1 32.63
CMD0	C5*	CMD16	C5*	
CMD1	A3_BA3	CMD17	A3_BA3	
CMD2	A2_BA0	CMD18	A2_BA0	
CMD3	A4_BA2	CMD19	A4_BA2	
CMD4	A5_BA1	CMD20	A5_BA1	
CMD5	WE*	CMD21	WE*	
CMD6	A7_A8	CMD22	A7_A8	
CMD7	A6_A11	CMD23	A6_A11	
CMD8	AB1*	CMD24	AB1*	
CMD9	A12_RFU	CMD25	A12_RFU	
CMD10	A0_A10	CMD26	A0_A10	
CMD11	A1_A9	CMD27	A1_A9	
CMD12	RS*	CMD28	RS*	
CMD13	RST*	CMD29	RST*	
CMD14	CKE*	CMD30	CKE*	
CMD15	CAS*	CMD31	CAS*	
GB2-64, GB28-64, GB48-128 Channel 0 & 1				
CMD32	Not used			
CMD33*	Reserved			
CMD34	DEBUG0†			
CMD35	DEBUG1†			

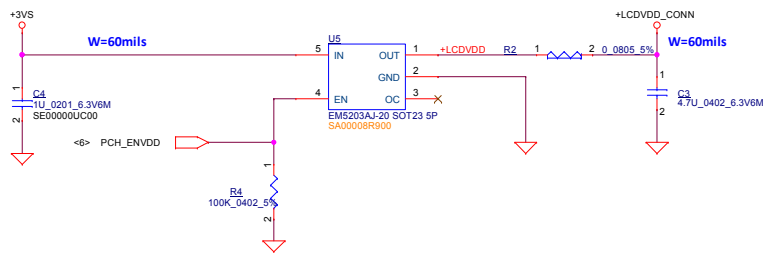
Notes:

1. Not available in GB2-64 and GB28-64 packages.
2. GPU debug pins; not connected to **UNAM**; see section 7.1.13.

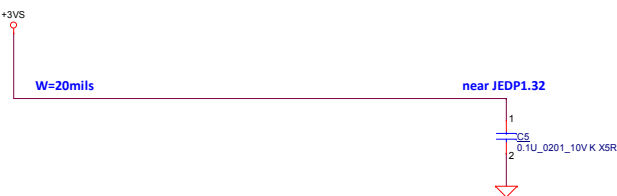
- Notes:
1. Not available in GB2-64 and GB2B-64 packages.
 2. GPU debug pins; not connected to UKAM. See section 7.1.13.



LCD POWER SWITCH



CAMERA POWER CIRCUIT

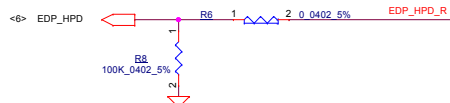


Vinafix.com

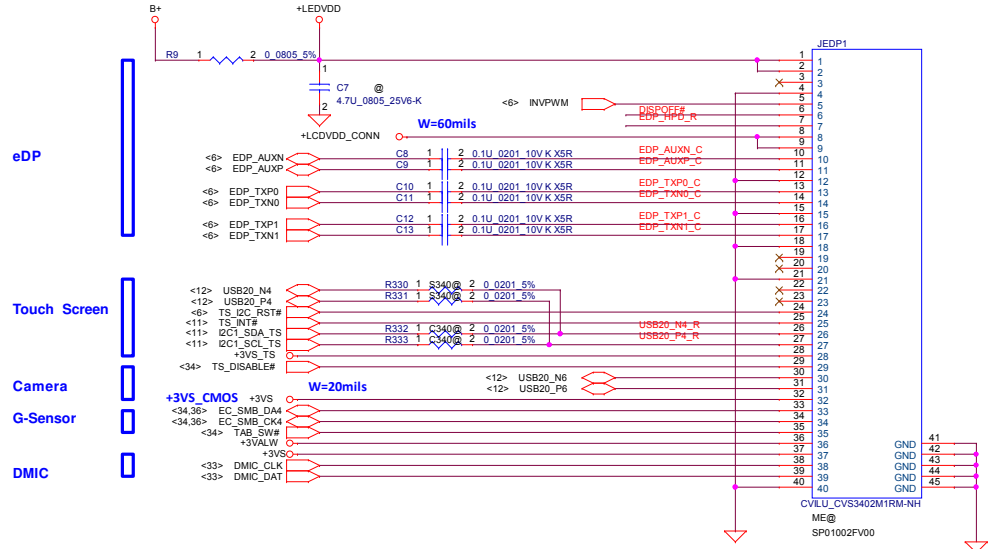
DISPLAY OFF



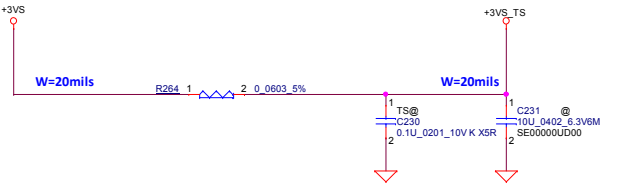
HOT PLUG DETECT

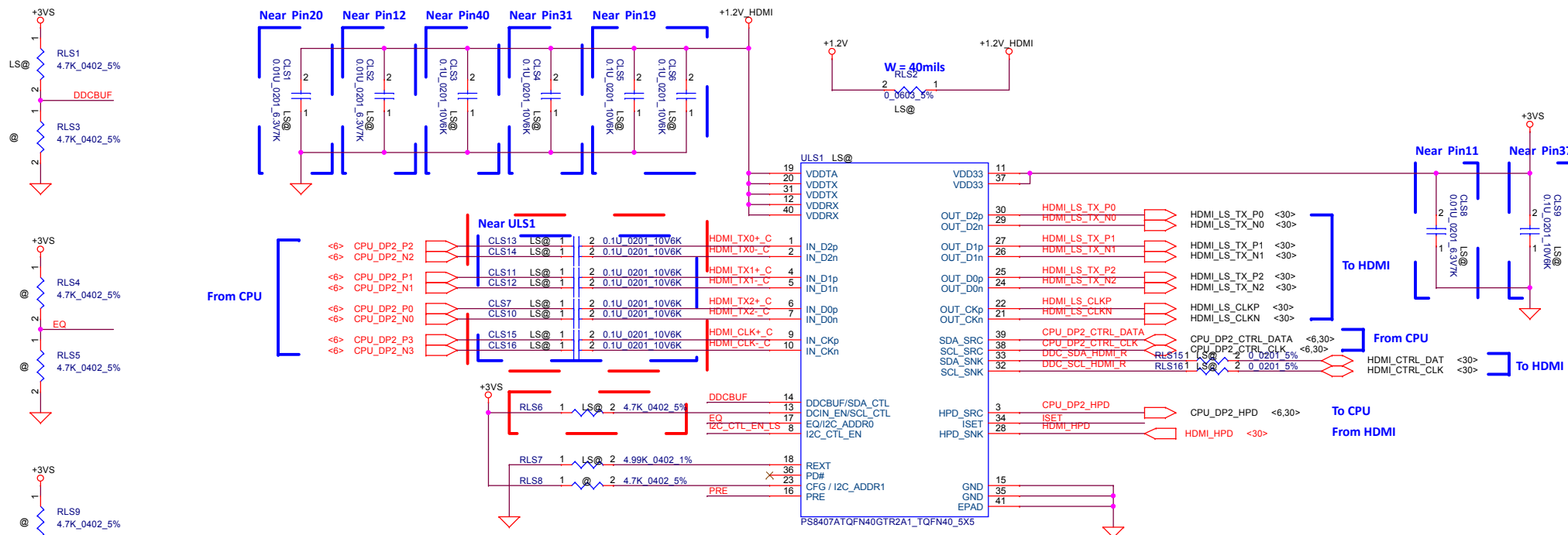


eDP CONNECTOR

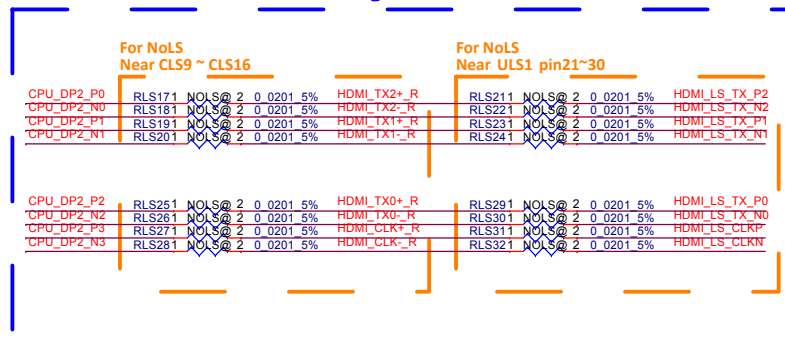


Touch Screen POWER CIRCUIT



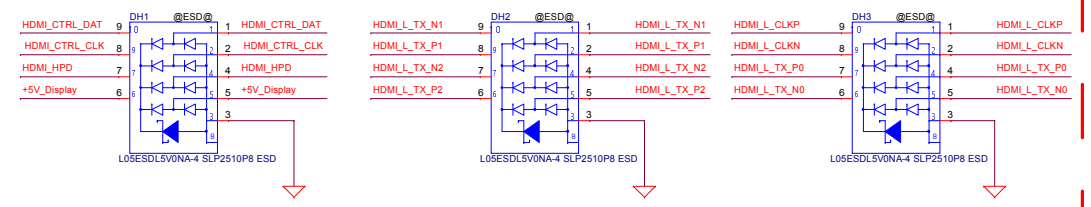
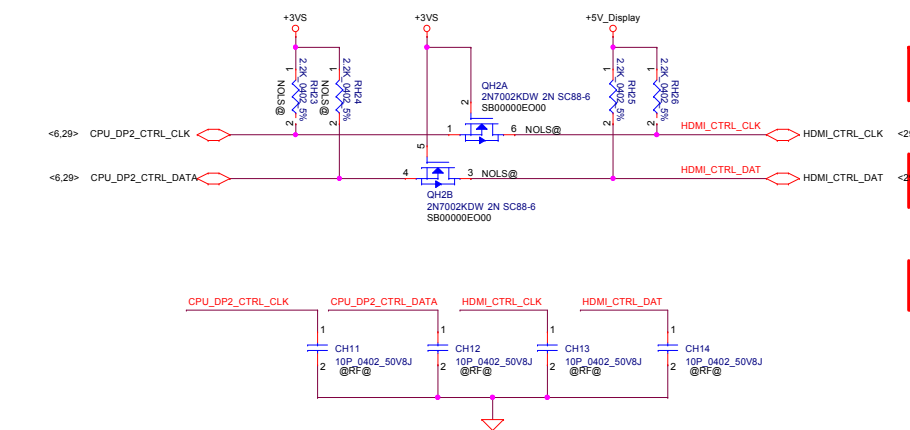
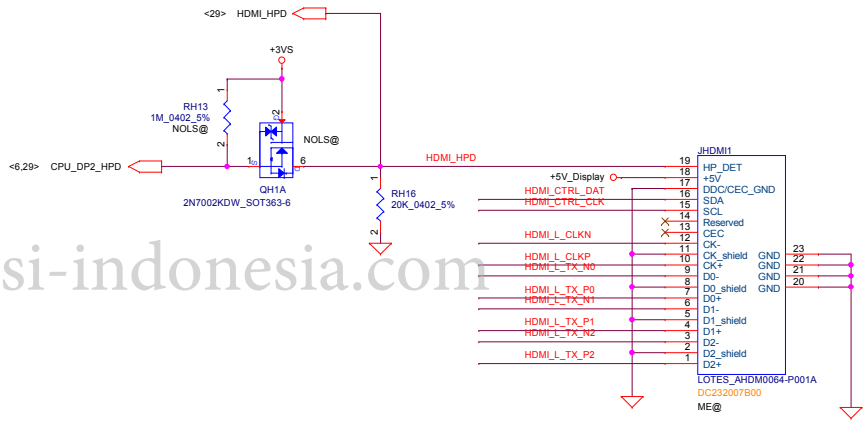
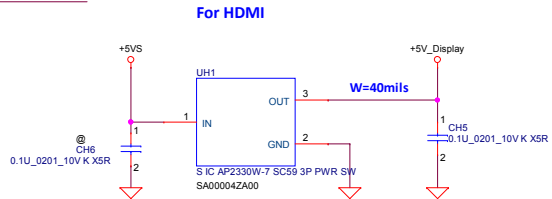
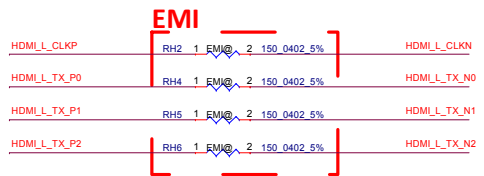
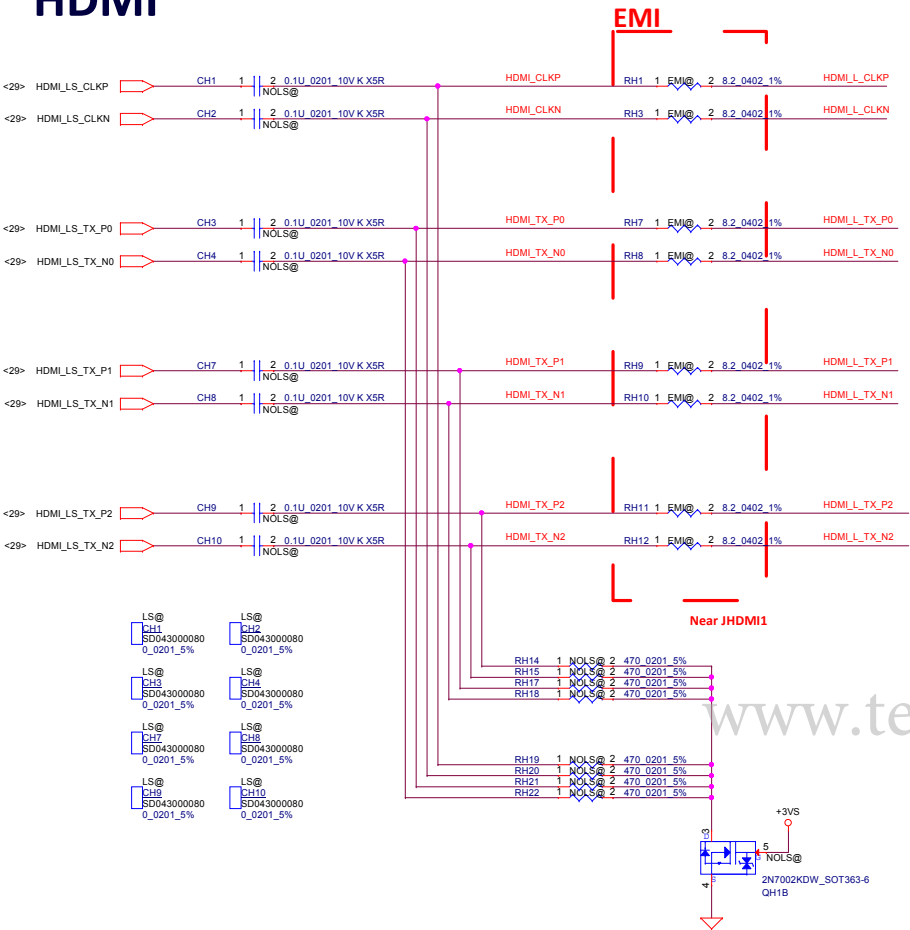


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Size	Document Number	Rev		LA-H101P	
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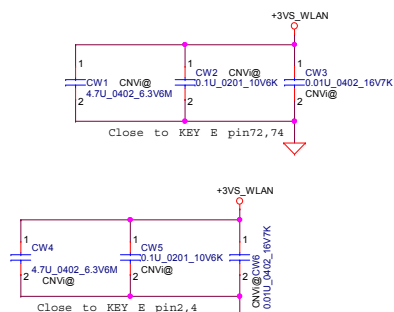
HDMI



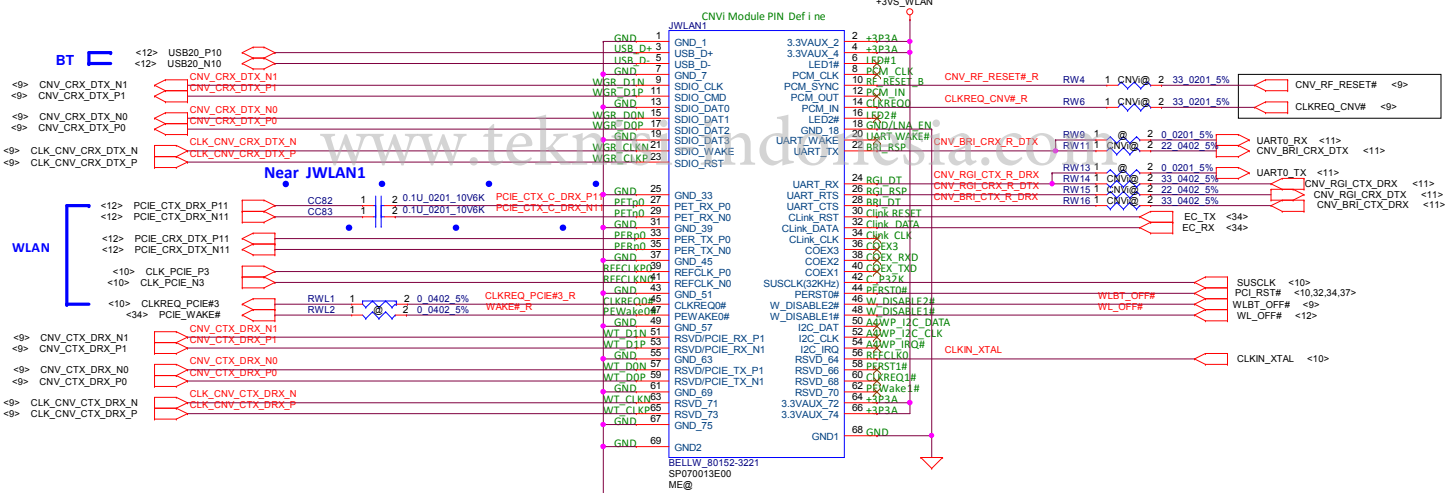
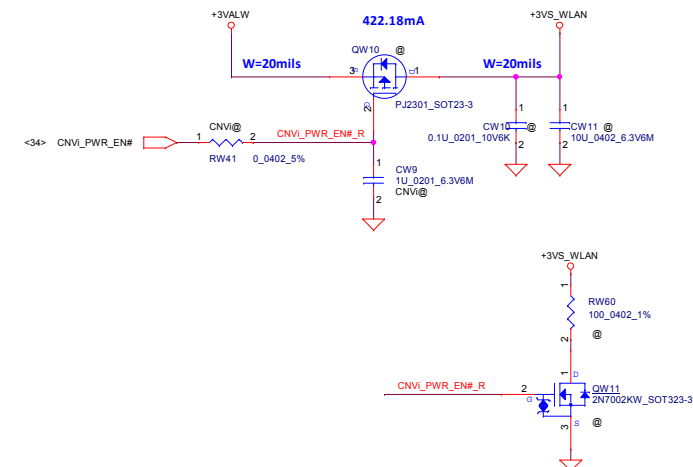
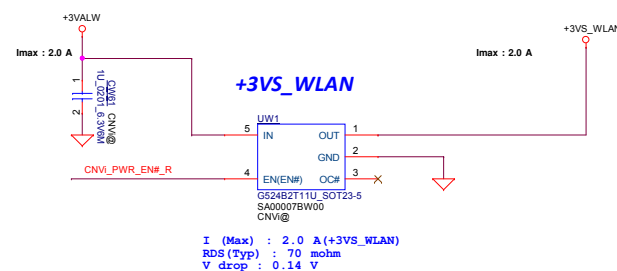
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NGFF WLAN /BT(Key E)

NGFF Wireless LAN / BT (Key E) [PCIE+USB/CNVi]

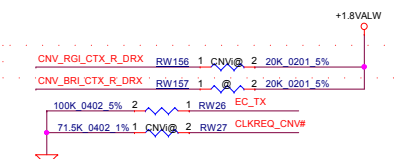


Jefferson Peak:1360mA@peak current
Thunder Peak 2:1100mA@peak current

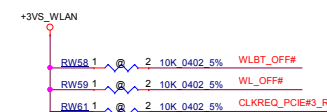


The connectivity module power supply pin shall be connected directly to the rail DSW.
From
567240 Intel Wireless AC 9560 Jefferson Peak EPS Rev1.1

PCH EDS : M.2 CNV Mode Select
GPP_F6/CNV_RGI_DT
 0 = Integrated CNVi enable.
 1 = Integrated CNVi disable.



Note: The real behavior of BT_DISABLE are
BT_DISABLE=LOW, BT=OFF
BT_DISABLE=HIGH, BT=ON

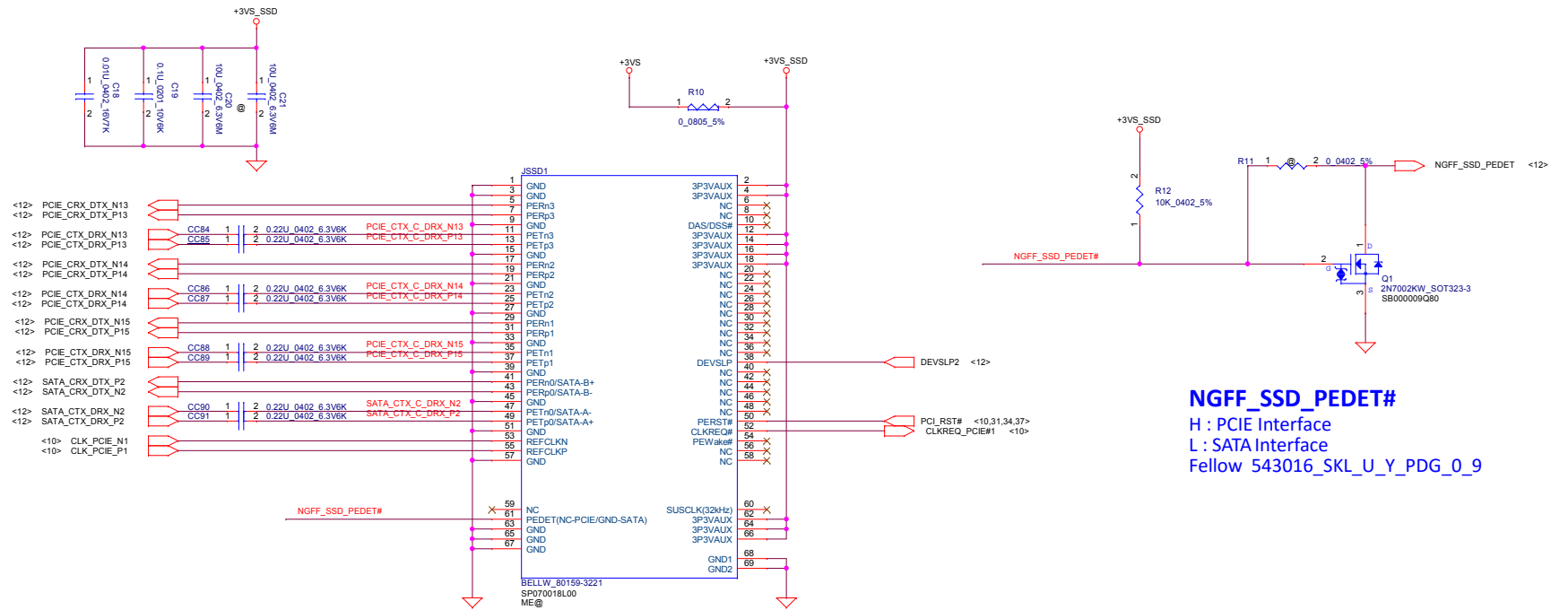


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				NGFF WLAN / BT		
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SSD(TYPE M)

SSD PCIE

SSD SATA



NGFF_SSD_PEDT#

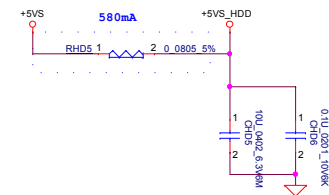
H : PCIE Interface

L : SATA Interface

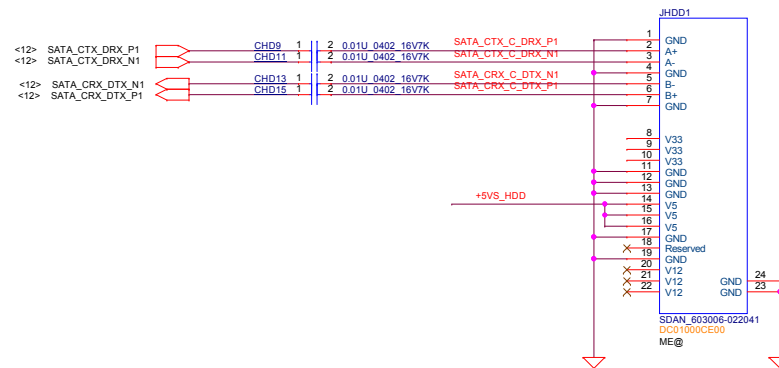
Fellow 543016_SKL_U_Y_PDG_0_9

SATA HDD

For Power consumption Measurement

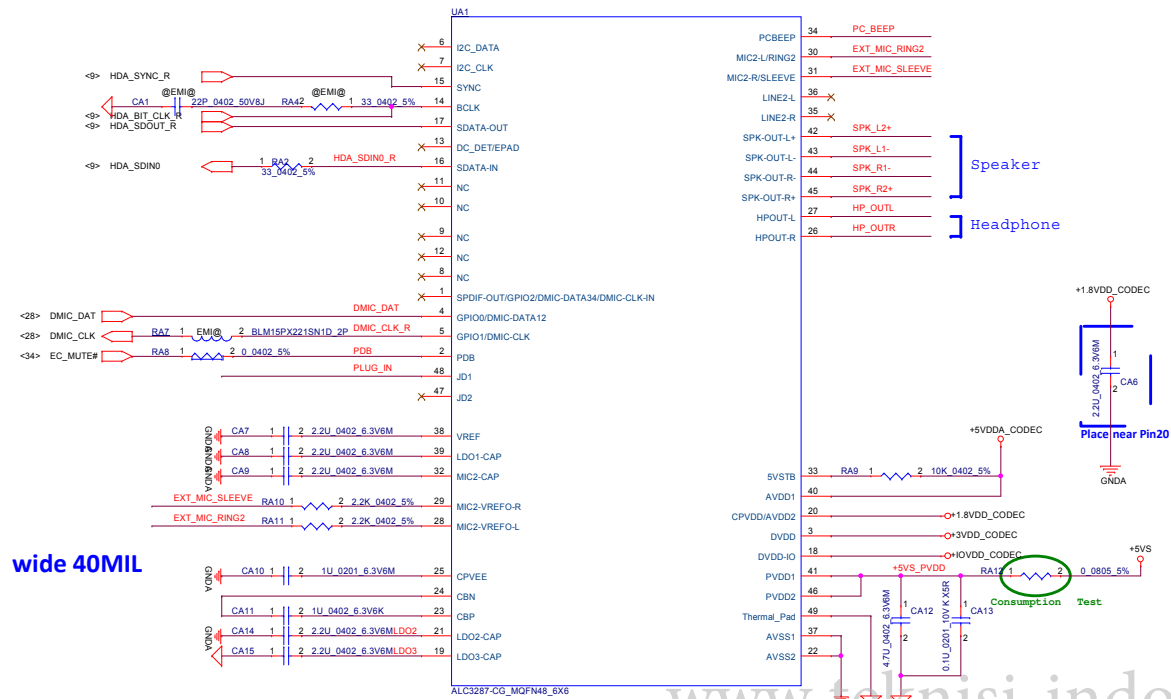


SATA HDD Conn.



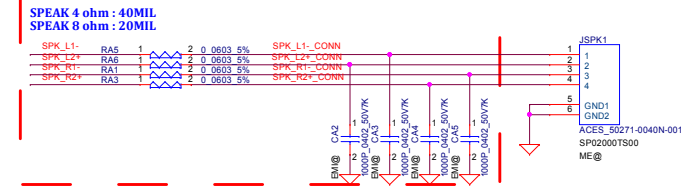
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				Document Number	0.A
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ALC3287



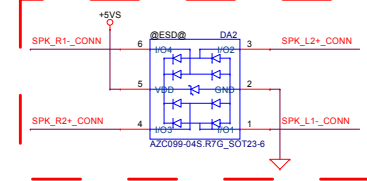
Speaker

FMT wide 40MIL

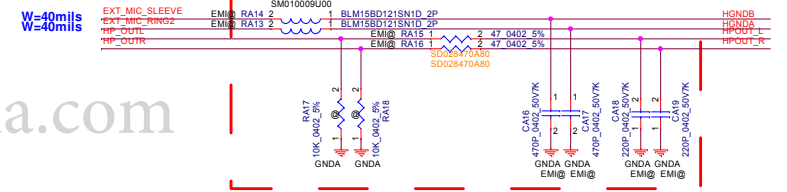


ESD protection needs to be placed near connector side

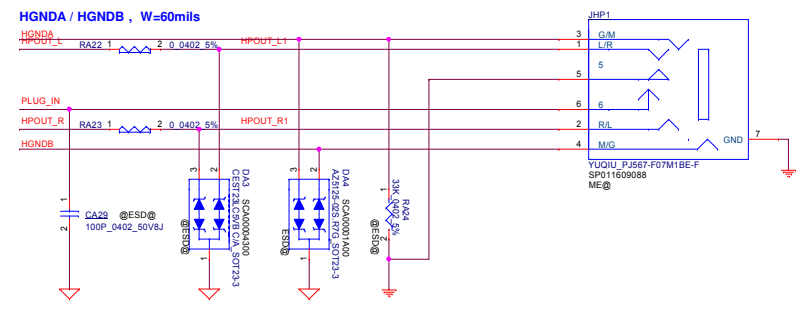
ESD



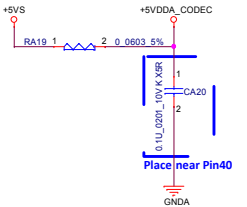
EMI



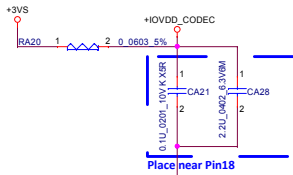
Combo Jack
(Normal Open)



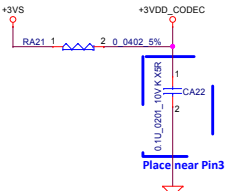
+5VS --> +5VDDA_CODEC



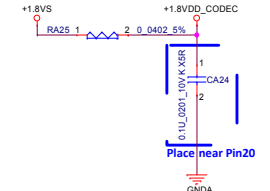
+3.3VS --> +IOVDD_CODEC



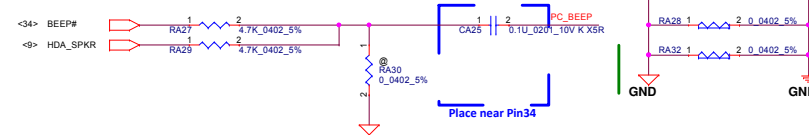
+3VS --> +3VDD_CODEC



+1.8VS --> +1.8VDD_CODEC



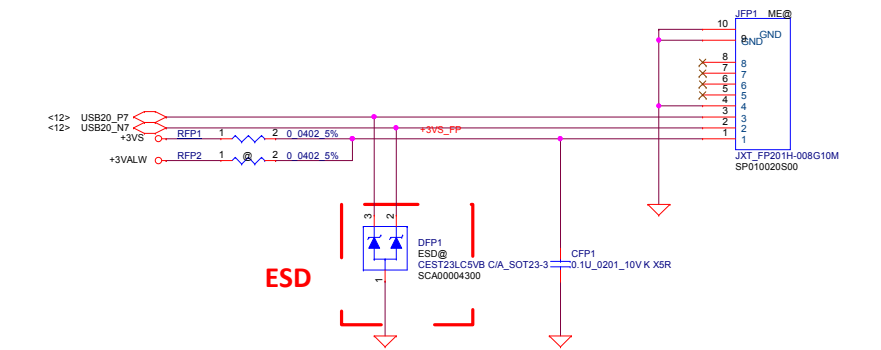
PC Beep



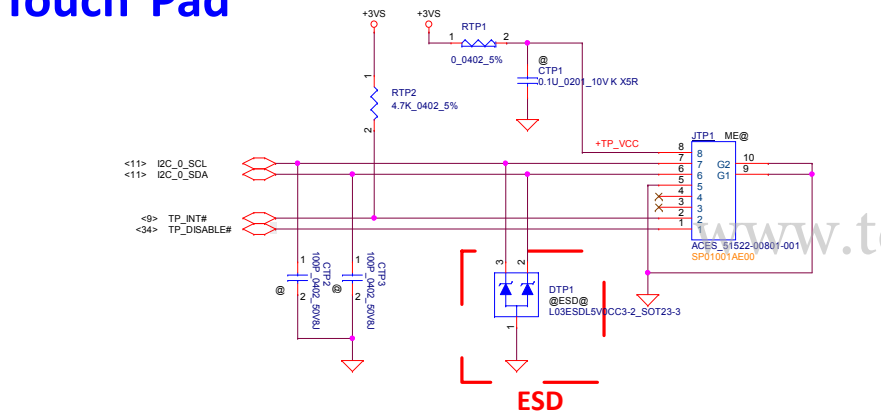
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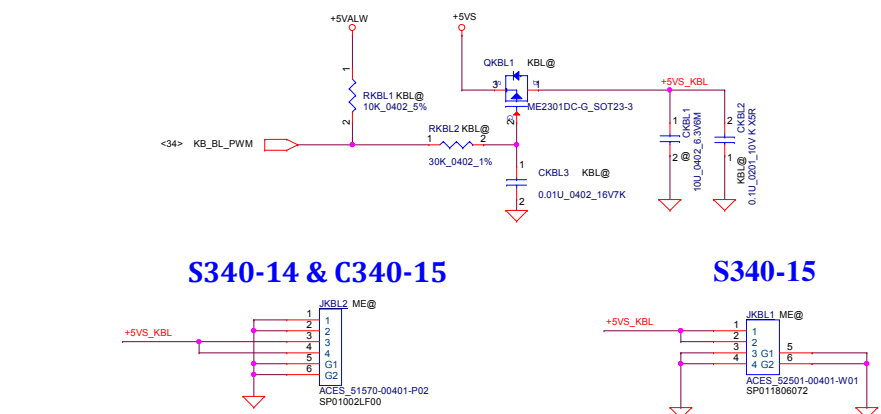
Finger printer



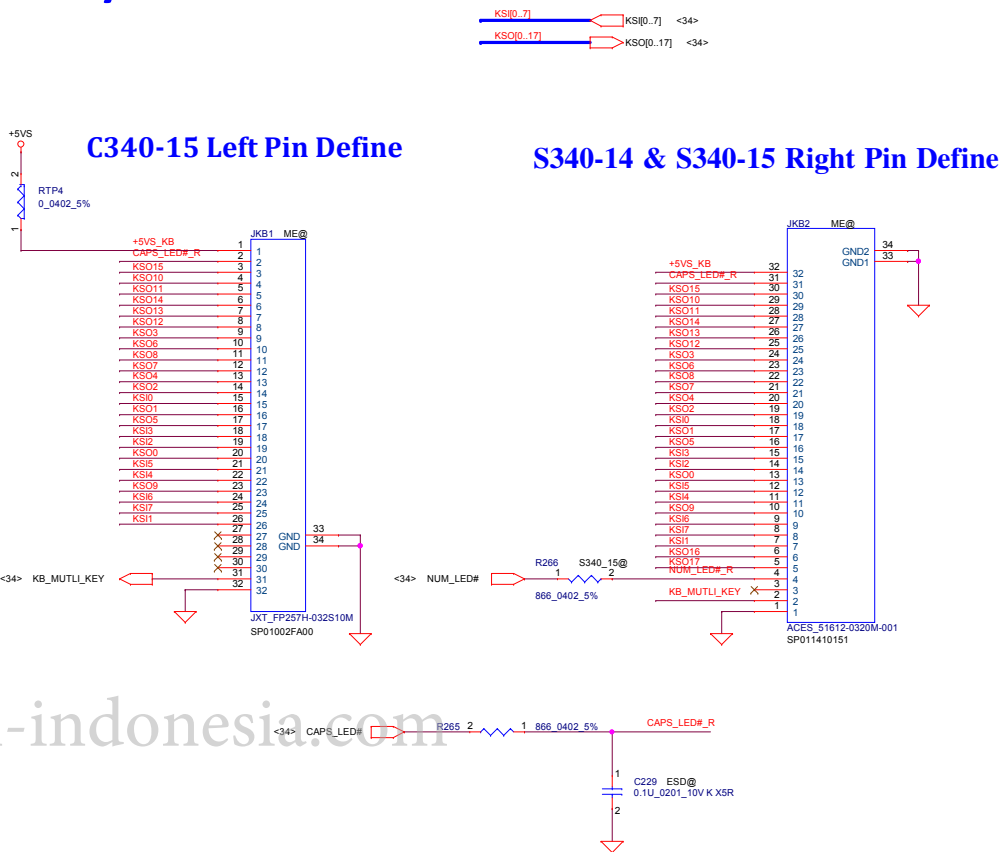
Touch Pad



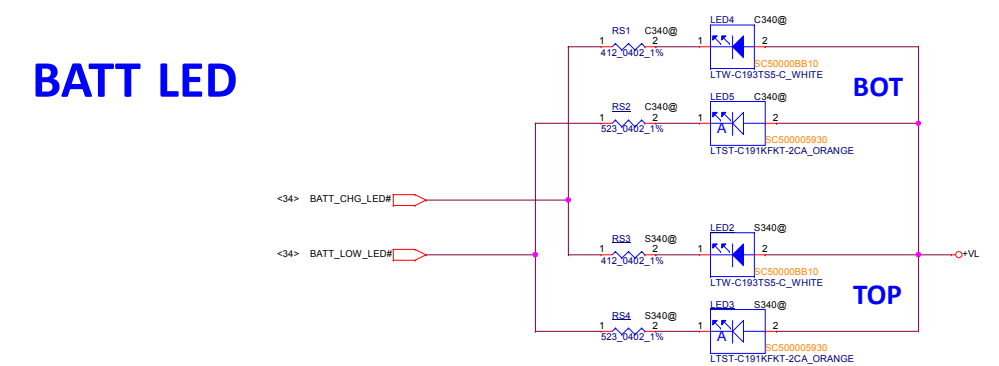
Keyboard Backlight



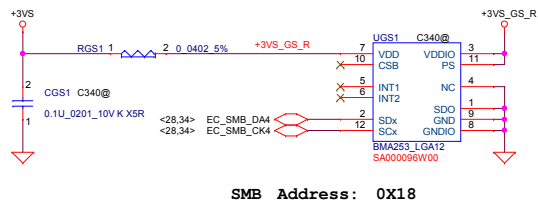
Keyboard



BATT LED

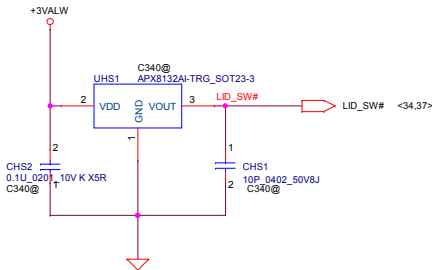


G-Sensor

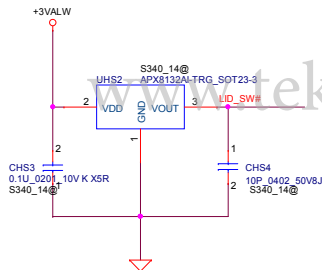


Hall Sensor

for C340

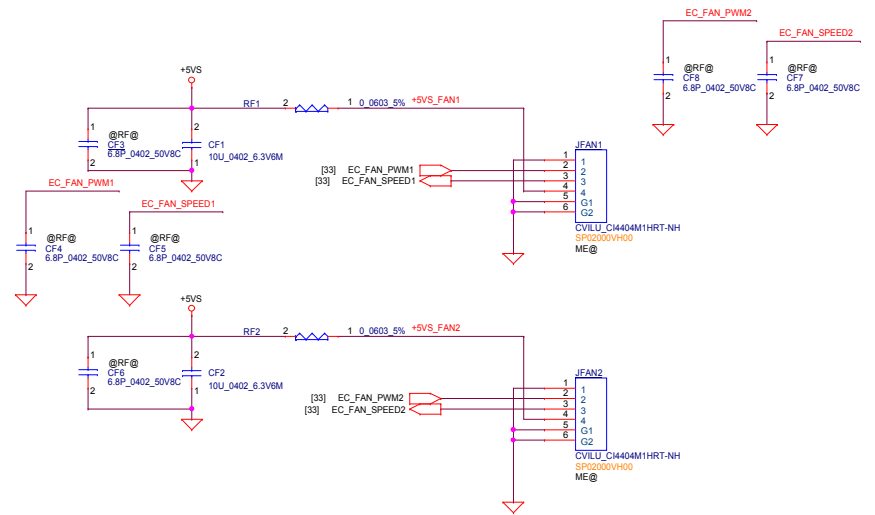


for S340 14"

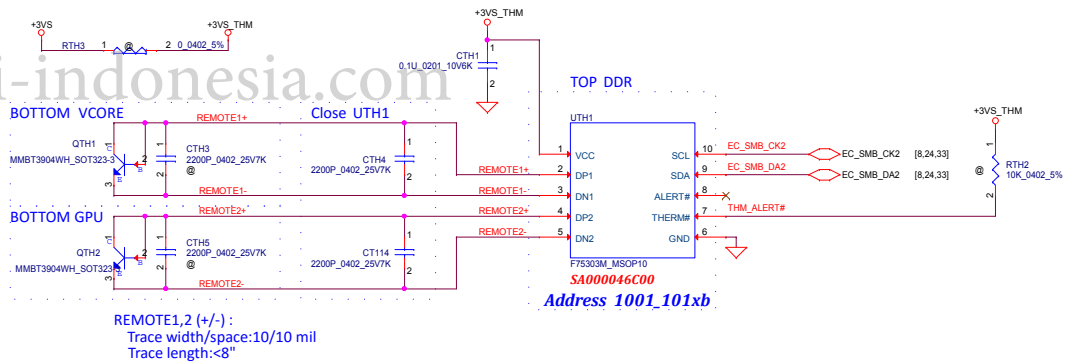


Thermal Sensor

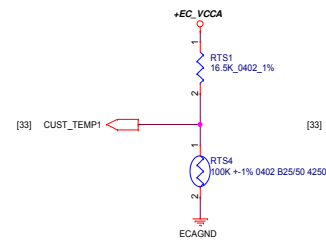
FAN



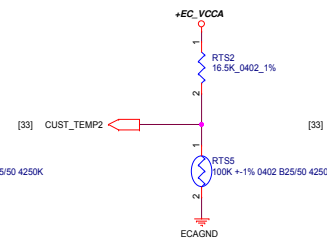
THERMISTOR



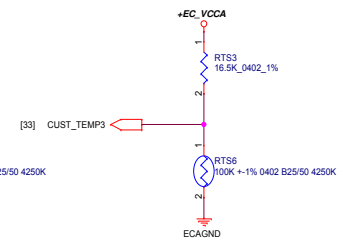
DDR4



GPU_CHOKE

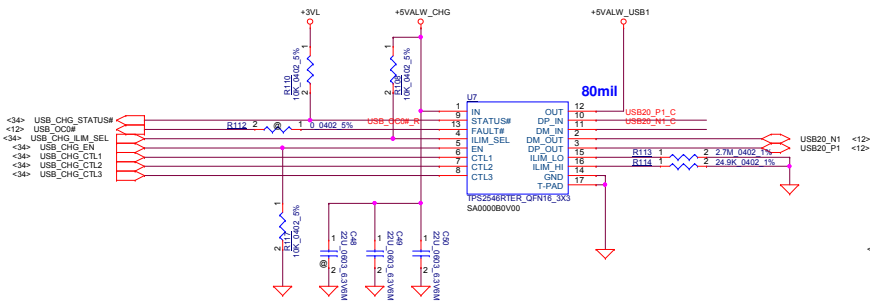


Charger CHOKE



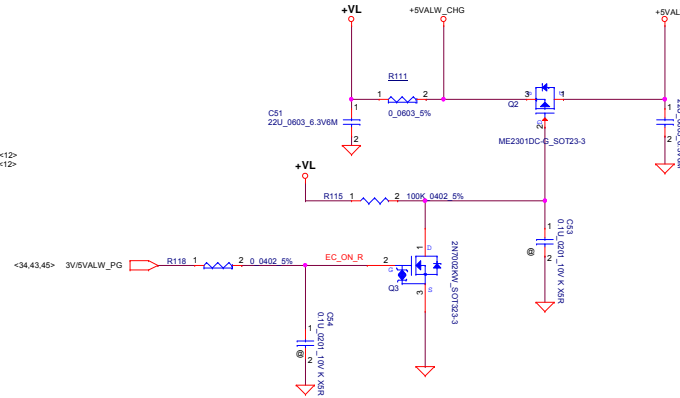
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Compal Electronics, Inc.				LA-H101P
FAN / Thermal Senser				0A
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USB3.0_Port (AOU_Port)

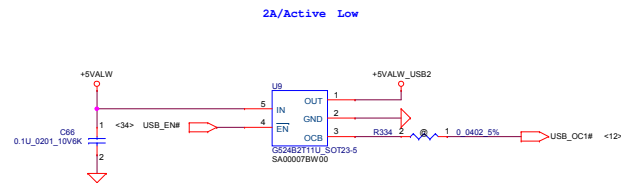


For USB Charger to improve +5VALWP power ripple

USB Charge switch



USB3.0_Port (Non-AOU_Port)

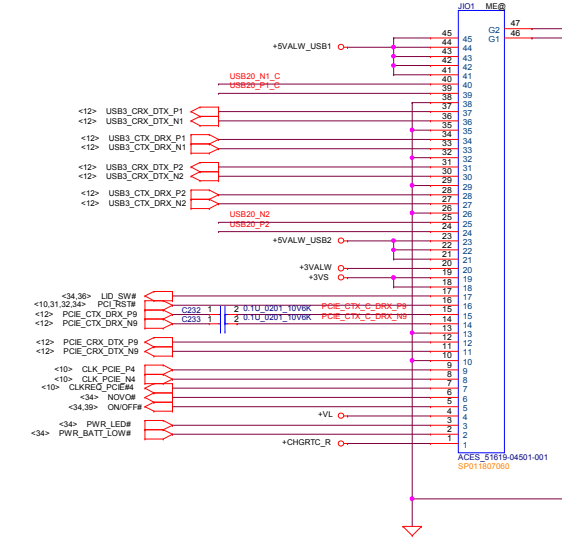


EMI



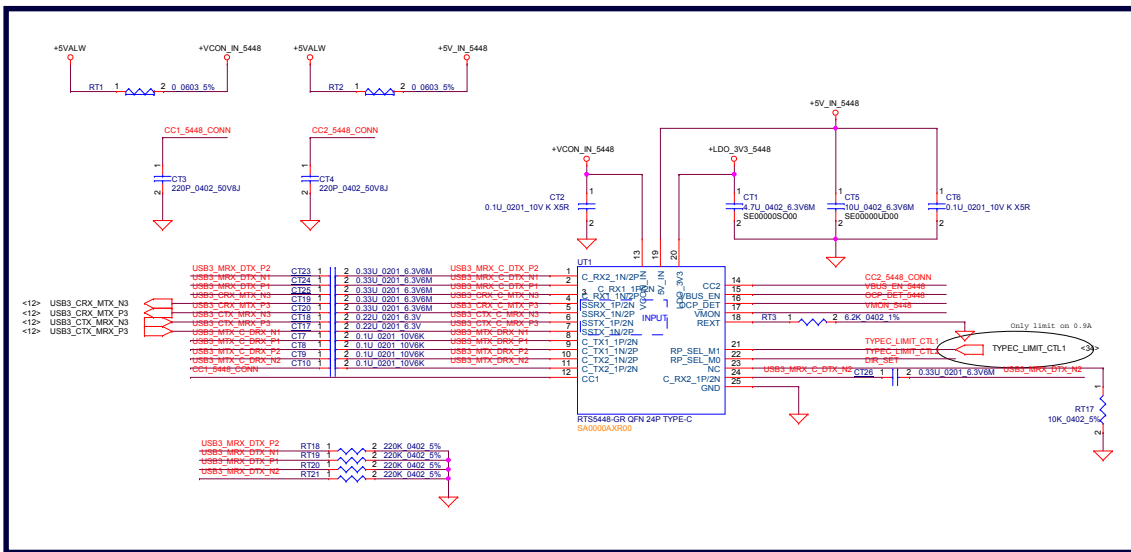
www.teknisi-indonesia.com

I/O CONN

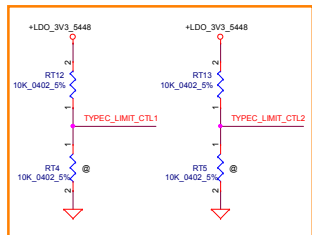


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								IO board		
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TYPE-C - CC+MUX (RTS5448-GR)

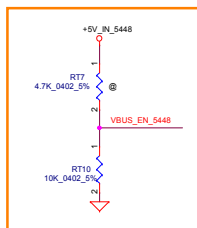
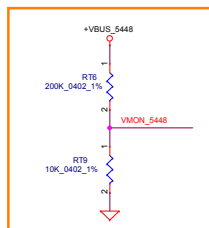


MUX MISC.

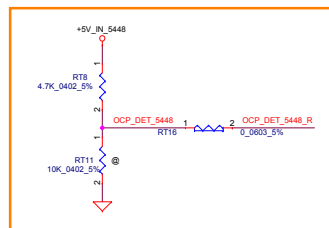


	M1	M0	Note
Rp:900mA	0	1	RT4/RT13 mount,RT12/RT5 don't mount
Rp:1.5A	1	0	RT12/RT5 mount,RT4/RT13don't mount
Rp:3.0A	1	1	RT12/RT13mount,RT4/RT5 don't mount

Rp Configuration



For C_VBUS
(Power Switch Enable Pin)

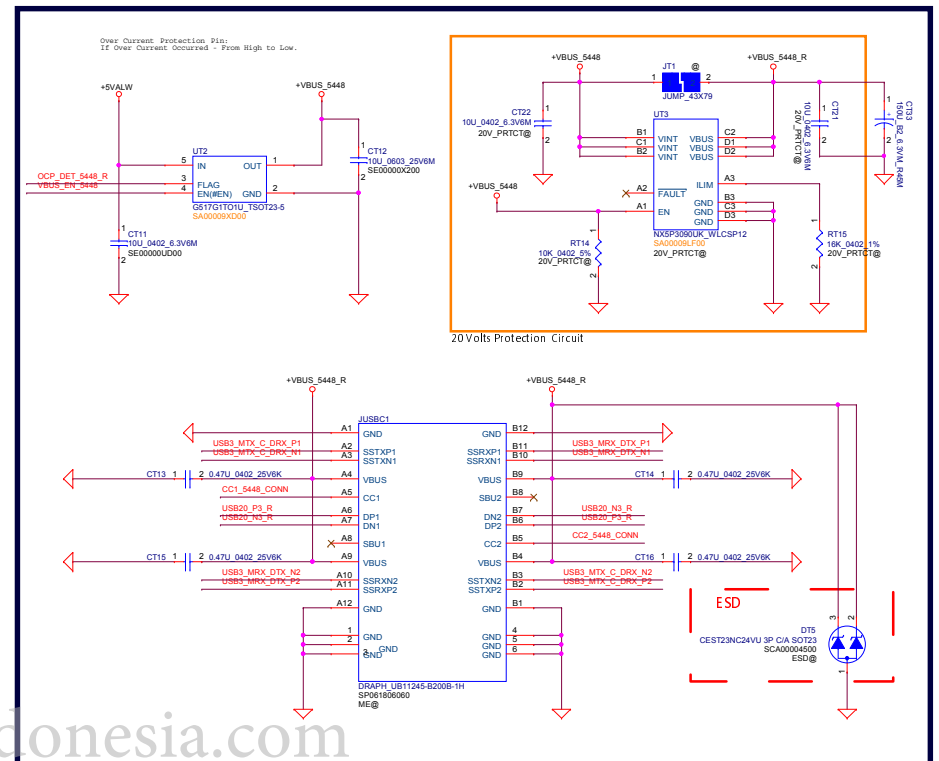


For C_VBUS
(Power Switch OCP Pin)

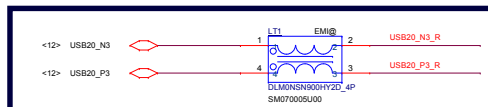
Power switch enable pin	Note
Low Active	RT7/RT10 mount
High Active	RT10 mount, RT7 don't mount

Power switch OCP pin	Note
Low Active	RT8/RT11 mount
High Active	RT11 mount, RT8 don't mount

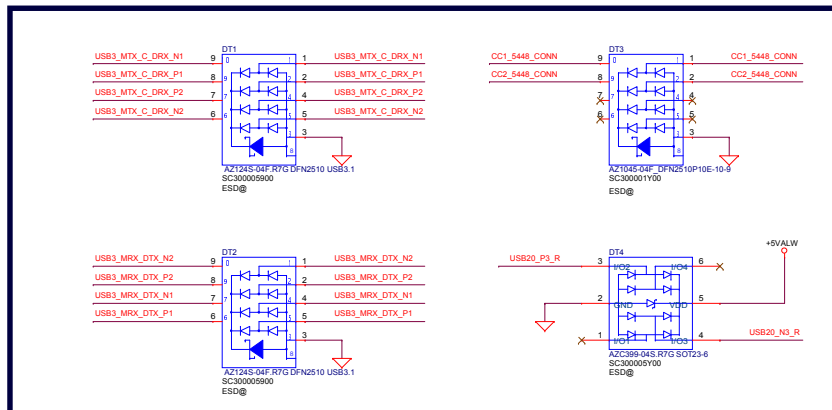
TYPE-C CONNECTOR



USB2.0

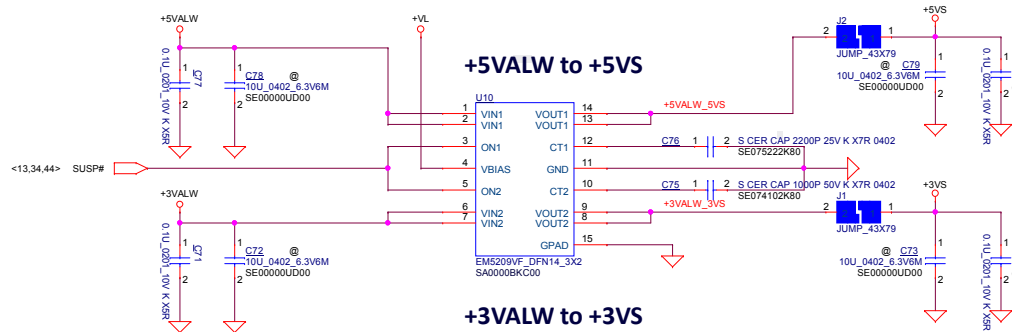


ESD COMPONENTS



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Date:	Thursday, September 20, 2018	(Sheet	38 of 51	

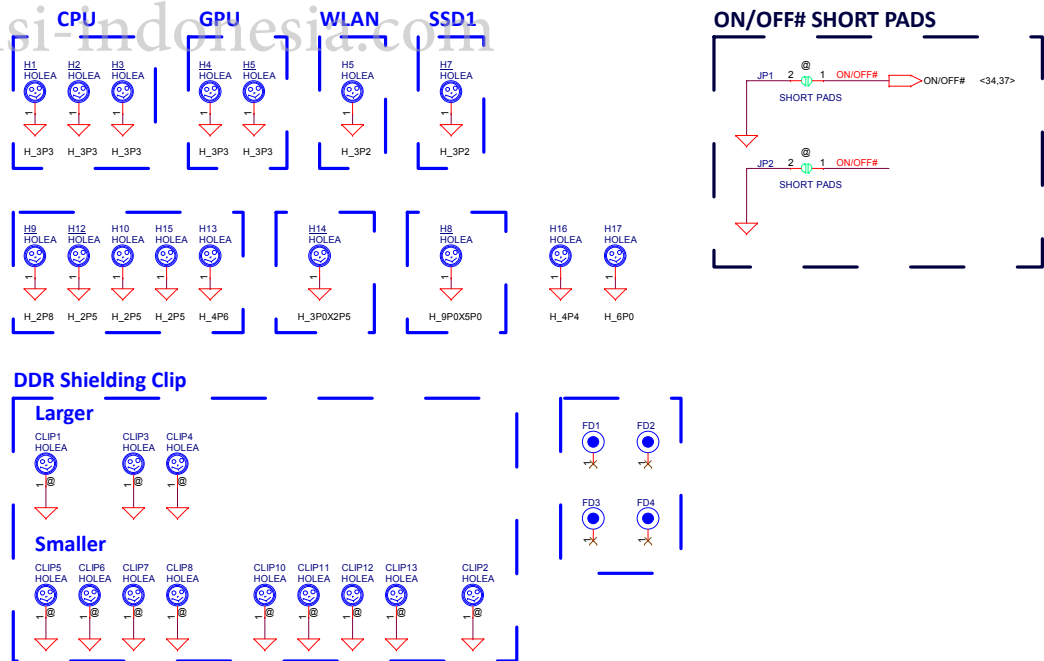
DC to DC



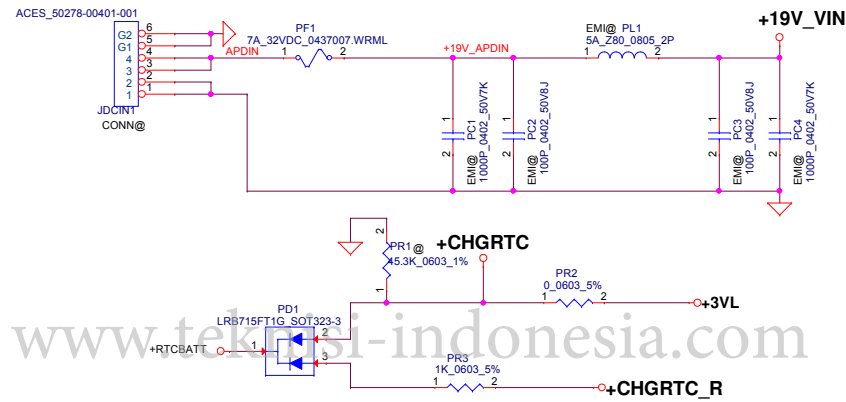
DISCHARGE CIRCUIT

For +1.8VALW Discharge

MISC.

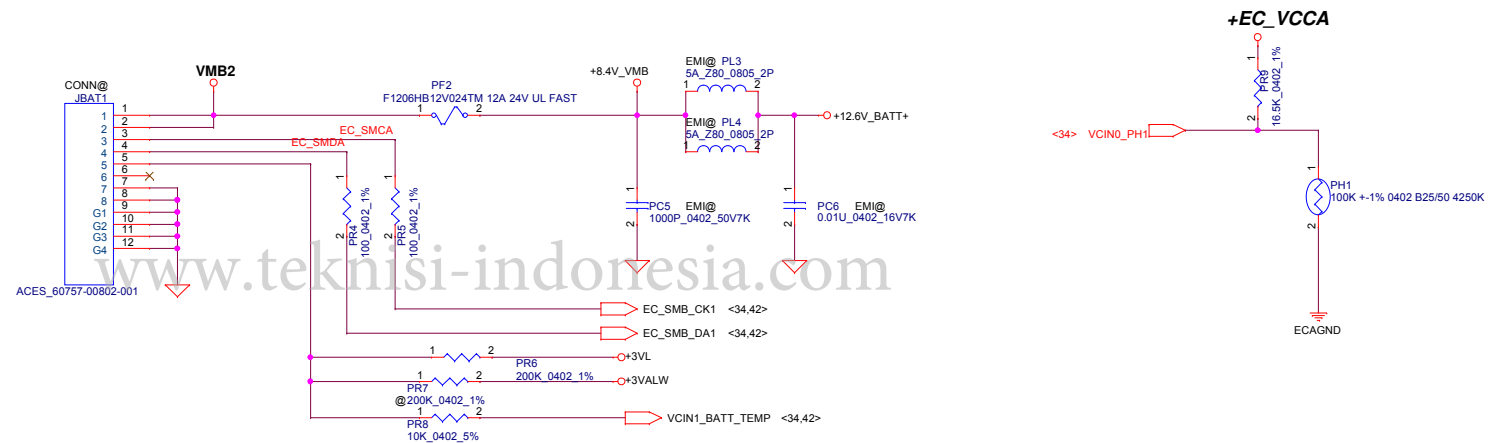


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				Date:	Thursday, September 20, 2018 Sheet 40 of 54

PH201 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C



Security Classification				Compal Secret Data				Compal Electronics, Inc.					
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										LA-H101P			
Date:				Thursday, September 20, 2018				Sheet 41 of 54					

Module model information
ISL95520A_Hybrid_Boost_V2.mdd

Protection for reverse input

Vgs = 20V
Vds = 60V
Id = 250mA

max Power loss 0.22W for 90W; 0.12W for 65W system; 0.05W for 45W
CSR rating: 1W
VCSIP-VCSIN spec < 81mV

Need check the SOA for inrush

PR729 and PR732 are ACDET set ting base on your project to set

0x3CH <BIT9> PSYS current gain
Rs1 = 10mΩ and Rs2 = 5mΩ or Rs1 = 10mΩ and Rs2 = 1mΩ
BIT0 = 1.14uA/W
BIT1 = 0.285uA/W
=====

Ipsys = KPSYS x (VAD P x IAD P + VBA T x IBAT)
R Psys = 1.2V / Ipsys
KPSYS = 1.14uA/W
adapter wattage = 45W
Battery wattage = 40Wh
Ipsys = 1.14 x (45+40) = 96.9uA
R Psys = 1.2V / 96.9uA = 12.3K-ohm.
=====

Design Notes
For 45W/65W /90W system, 2S/3S/4S battery
Maximum Charging current 3.5A
Maximum Battery discharge power 55W
#Register Setting
1. 0X3DH bit10 set 0 (default 1) to enable turbo boost function
2. Disable turbo when AC only
#Circuit Design
1. ACLIM and CCLIM are divider voltage control.
2. Use 7X7 choke and 3X3 H/L side MOSFET
Charge current 3A
Power loss : 1.79W (H/S=0.227W, L/S=1.2738W, Choke=0.297W)
Power density : 0.61 (23X16)
#Protect function
1. AC0VP : VCC voltage > 24V
2. SMBus timeout : 0X3DH bit15 set 0 (default 0) to enable 175s(default).
3. ACOC : 0X3CH bit4 set1 release adapter limit function (default:Enable).
4. CHOCOP : based on charge current setting
5. BAT0VP : 4.6V/Cell
6. BATLOW : No.
7. TSHUT : 150C

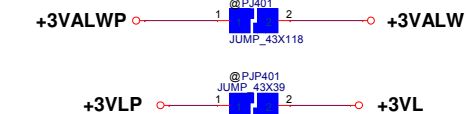
(Rs1 = 10mΩ and Rs2 = 5mΩ or Rs1 = 20mΩ and Rs2 = 10mΩ).
CC_LIM = VccLIM / 64 x Rs2
=====

Battery current limited by CCLIM ~ 3.89A.
Adapter current limited by ACLIM ~ 4.33A.
(PR719 and PQ741 are for change ACLIM when AC in)

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Security Classification		Compal Secret Data		Title	
Issued Date	2014/11/05	Deciphered Date	2014/12/15	PWR_CHARGER	
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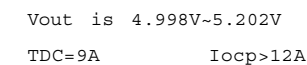
SY8286B_V3_single.mdd
SY8286B_V3_dual.mdd



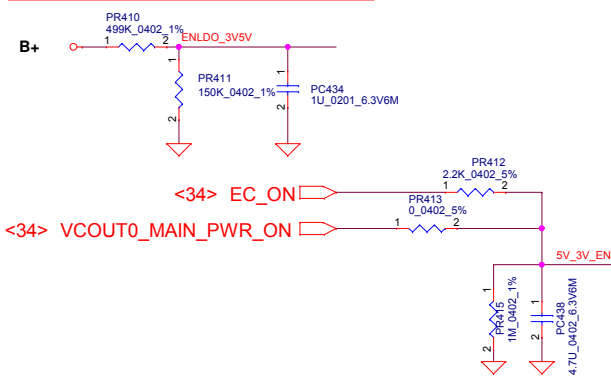
```
Fsw : 600K Hz
EN1 and EN2 dont't be floating.
EN :H>0.8V ; L<0.4V
```

keep short pad,
snubber is for EMI only.

Vinafix.com



SY8286C_V3_single.mdd
SY8286C_V3_dual.mdd



```
EN1 and EN2 dont't be floating.
EN :H>0.8V ; L<0.4V
```

Fsw : 600K Hz

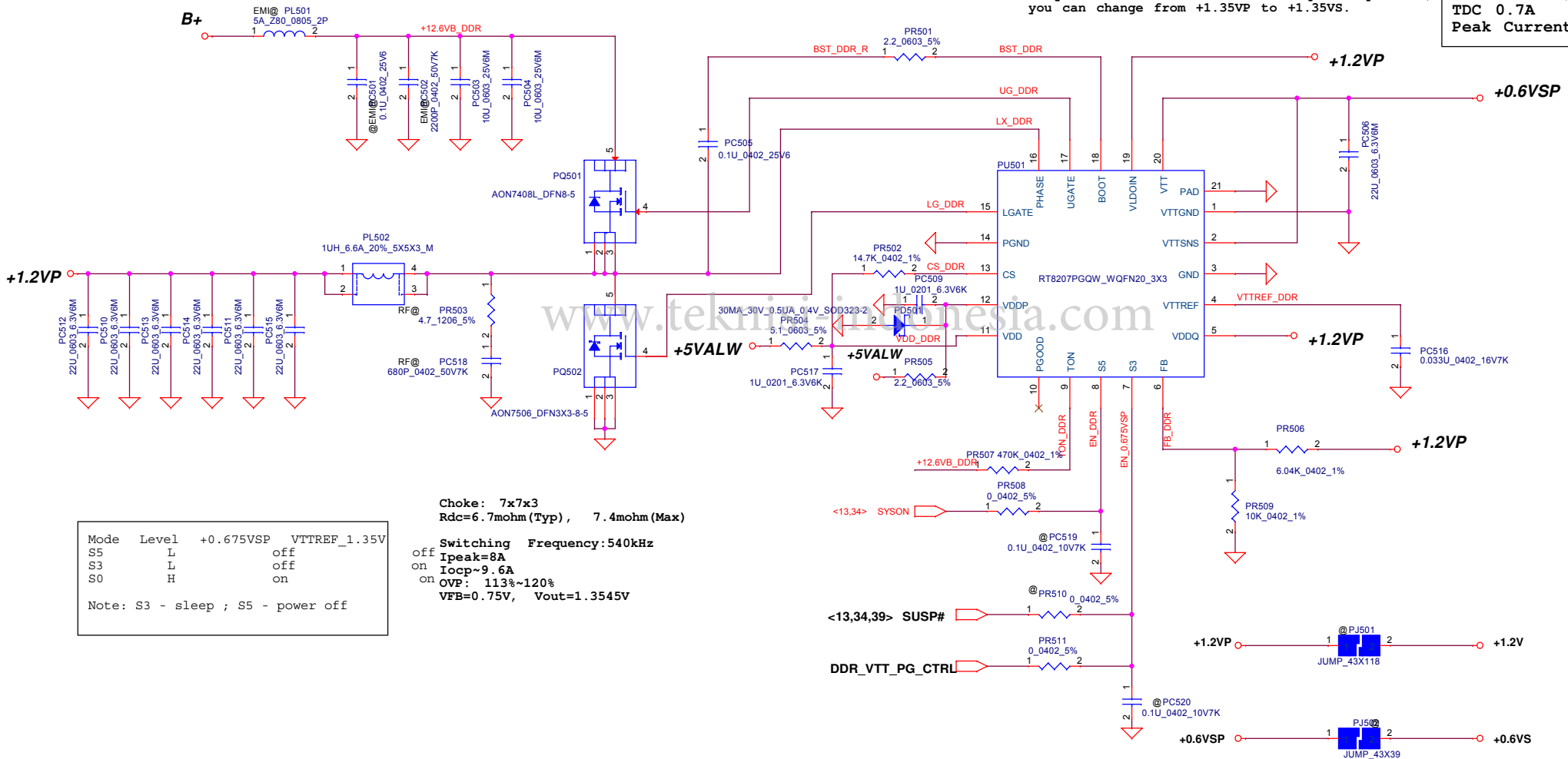
Security Classification		Compal Secret Data		<i>Compal Electronics, Inc.</i> +3VALW/+5VALW	
Issued Date	2018/04/09	Deciphered Date	2019/04/09	Title	
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Module model information

RT8207P_single_V3.mdd For Single layer
RT8207P_dual_V3.mdd For Dual layer

Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question,
you can change from +1.35VP to +1.35VS.

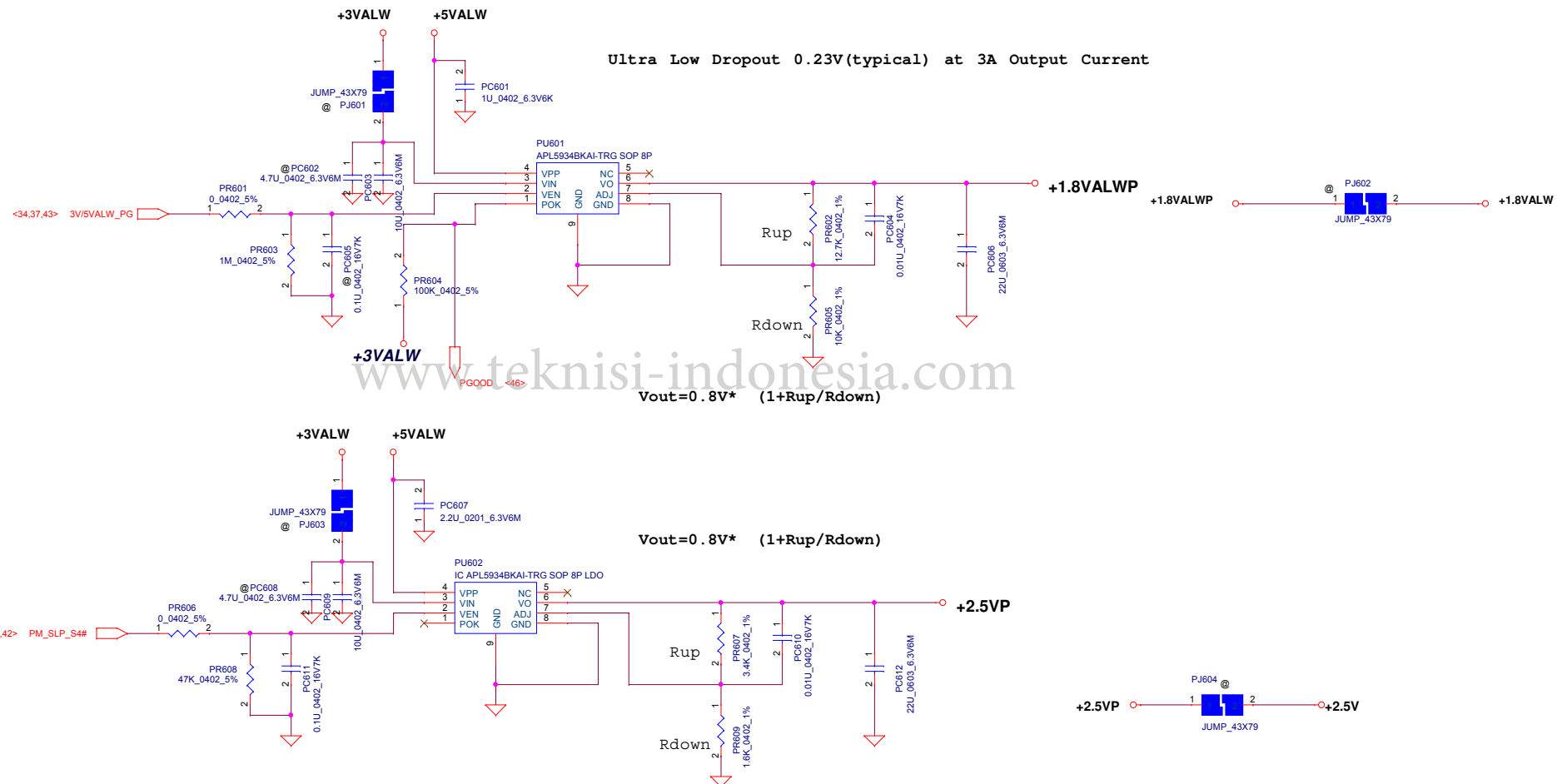
0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A



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				Custom	LA-H101P
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Module model information

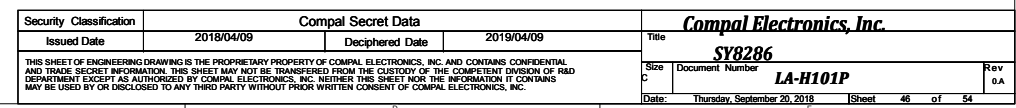
APL5930_V2.mdd



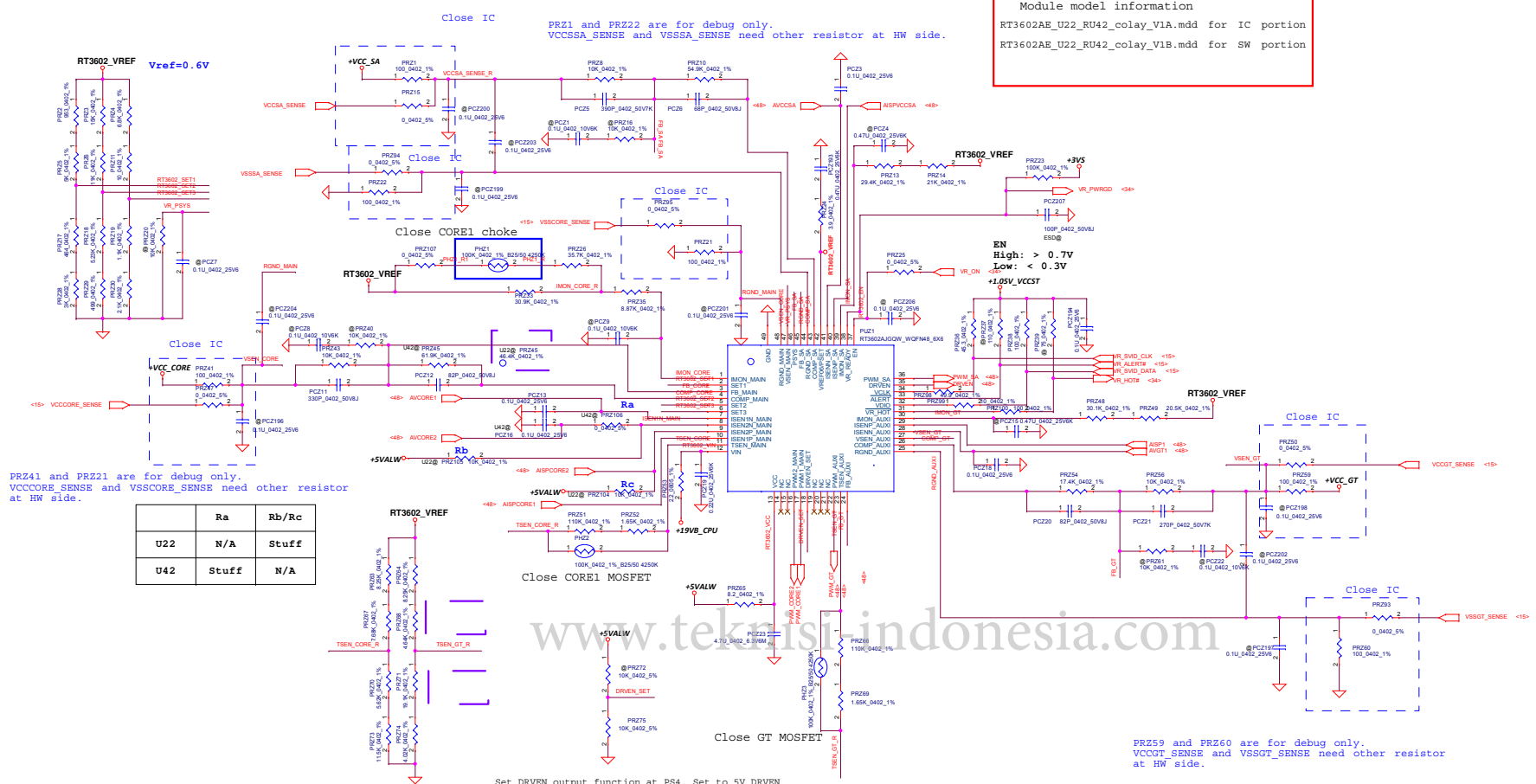
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Issued Date	2018/04/09	Deciphered Date	2019/04/09	Title	APL5930
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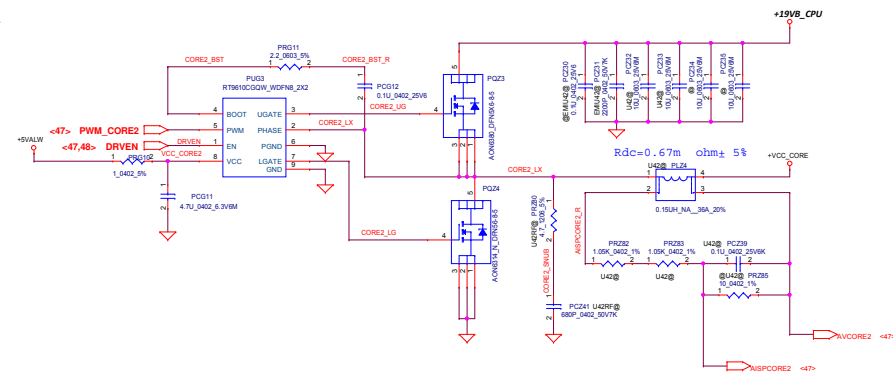
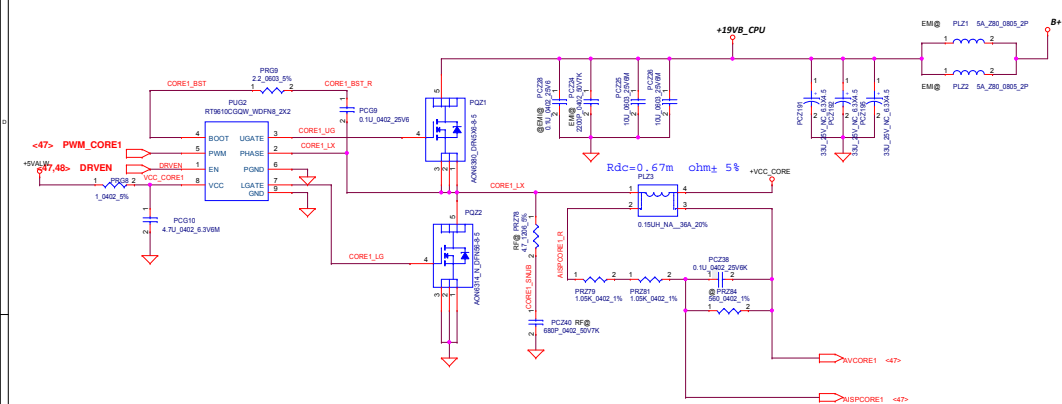
Vinafix.com

keep short pad,
snubber is for EMI only.



Module model information
 RT3602AE_U22_RU42_colay_V1A.mdd for IC portion
 RT3602AE_U22_RU42_colay_V1B.mdd for SW portion





H/S AON6280:
 R DS (ON) (at V GS =10V) < 6.8m
 R DS (ON) (at V GS =4.5V) < 10.5m
 L/S AON6214:
 R DS (ON) (at V GS =10V) < 2.8m?
 R DS (ON) (at V GS =4.5V) < 3.5m?

VCC_CORE
 FSW=450kHz
 Choke=0.15uH
 DCR=0.67 mohm +/- 5%

VCC_GT
 FSW=450kHz
 Choke=0.15uH
 DCR=0.67 mohm +/- 5%

VCC_SA
 FSW=600kHz
 DCR=6.2 mohm +/- 5%

U22
 LI=2.4 mohm
 TDC=21A
 ICCMAX=32A
 OCP=40A

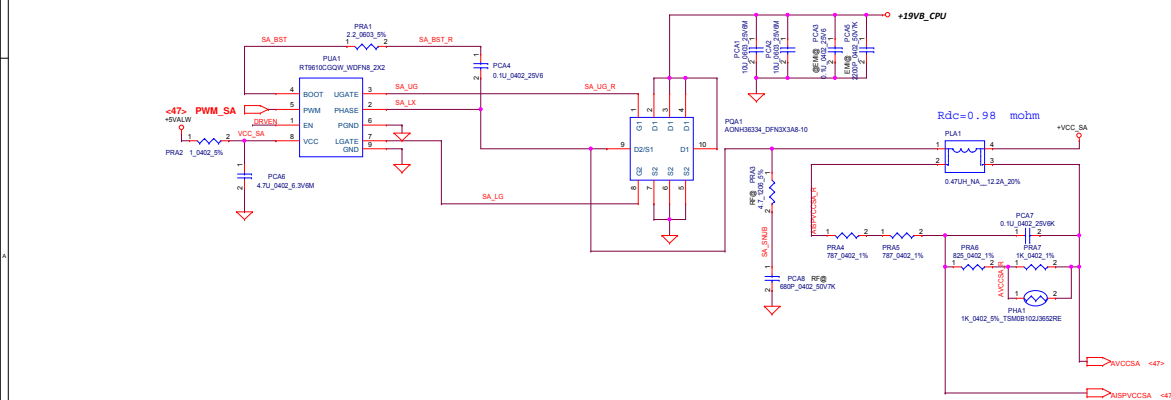
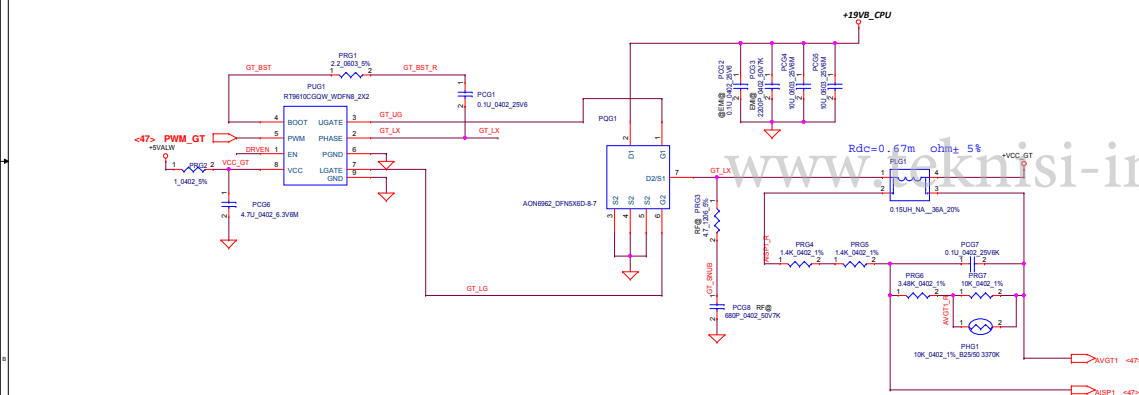
U22
 LI=3.1 mohm
 TDC=18A
 ICCMAX=31A
 OCP=39A

U22
 LI=10.3 mohm
 TDC=4A
 ICCMAX=5A
 OCP=10A

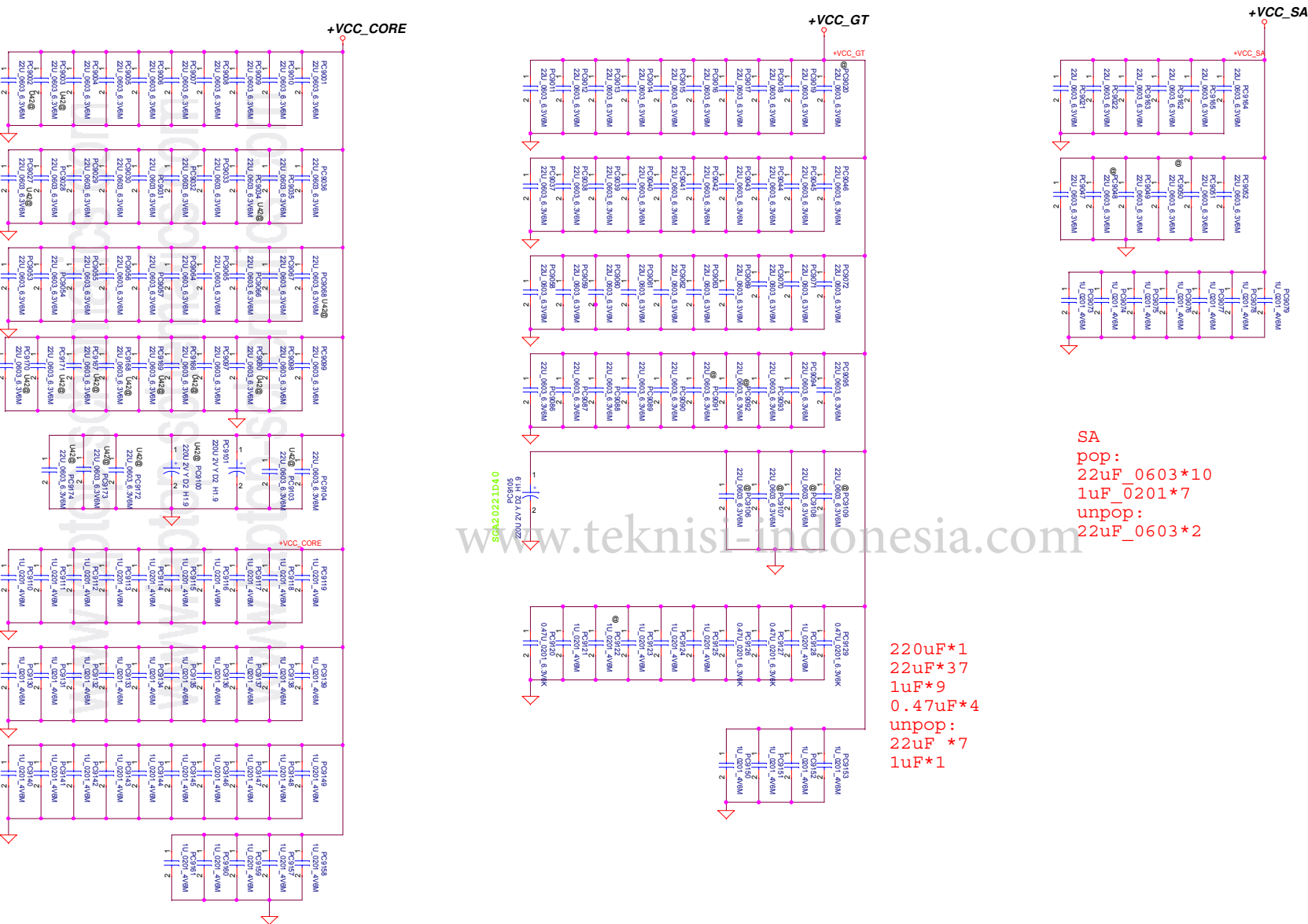
U42
 LI=2.4 mohm
 TDC=42A
 ICCMAX=64A
 OCP=70A

U42
 LI=3.1 mohm
 TDC=12A
 ICCMAX=28A
 OCP=39A

U42
 LI=10.3 mohm
 TDC=4A
 ICCMAX=5A
 OCP=10A



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				CPU Power stage	
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SA
pop:
22uF_0603*10
1uF_0201*7
unpop:
22uF_0603*2

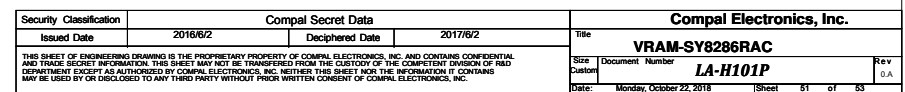
220uF*1
22uF*37
1uF*9
0.47uF*4
unpop:
22uF *7
1uF*1

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2018/08/15
VCORE Output Capacitor:
U42
22uF_0603*41
1uF_0201*35
220uF *2
UNPOP
22_0603*1

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				Power Train					
				Size C	Document Number		LA-H101P		Rev
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SY8286_V1_single.mdd
SY8286_V1_dual.mdd



Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					
18					

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				Date:	Thursday, September 20, 2018	Sheet 53 of 61